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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT

SAN FRANCISCO DIVISION

SEMICONDUCTOR ENERGY LABORATORY COMPANY, LTD.,

Plaintiff,

vs.

ACER INCORPORATED, ACER AMERICA CORPORATION, and AU OPTRONICS CORPORATION,

Defendants.

CASE NO. C 02-02800 WHA

ACER INCORPORATED AND ACER AMERICA CORPORATION'S PRELIMINARY PROPOSED CONSTRUCTIONS OF IDENTIFIED CLAIM TERMS

Pursuant to Patent Local Rule 4-2(a), Acer Incorporated and Acer America Corporation (collectively "Acer") hereby submits its preliminary proposed construction of each claim term, phrase, or clause which the parties collectively have identified for claim construction purposes pursuant to Patent Local Rule 4-1.

I. U.S. PATENT NO. 6,355,941

Claim term	Acer's preliminary proposed construction	Extrinsic evidence
Non-single crystal semiconductor	"Non-single crystal semiconductor" means "semiconductor material having lattice strain."	
Intrinsic	"Intrinsic" means that the non-single crystal semiconductor material has the charge-carrier concentration of a pure, ideal crystal of that material.	"A semiconductor whose charge-carrier concentration is substantially the same as that of the ideal crystal." *IEEE Standard Dictionary of Electrical and Electronics Terms*, Sixth Edition.
Channel region	"Channel region" means "the surface current path connecting the source and drain regions."	"A surface layer of carriers connecting source and drain in an insulated-gate field-effect transistor." *IEEE Standard Dictionary of Electrical and Electronics Terms*, Sixth Edition.

II. U.S. PATENT NO. 6,404,480

Claim term	Acer's preliminary proposed construction	Extrinsic evidence
Second interlayer insulating film having at least two openings	The term "at least two openings" means "two holes in the contact structure located in the common contact portion."	

III. U.S. PATENT NO. 5,929,527

Claim term	Acer's preliminary proposed construction	Extrinsic evidence
The film made of aluminum or a material containing aluminum as a principal component contains oxygen atoms at a concentration of $8x10^{18}$ atoms·cm^{-3} or less, carbon atoms at a concentration of $5x10^{18}$ atoms·cm^{-3} or less, and nitrogen atoms at a concentration of $7x10^{17}$ atoms·cm^{-3} or less	This phrase means "the maximum concentration of oxygen cannot exceed $8x10^{18}$ atoms·cm^{-3} at any point in the thin film containing aluminum as a principal component, the maximum concentration of carbon cannot exceed $5x10^{18}$ atoms·cm^{-3} at any point in the thin film containing aluminum as a principal component, and the maximum concentration of nitrogen cannot exceed $7x10^{17}$ atoms·cm^{-3} at any point in the thin film containing aluminum as a principal component."	

IV. U.S. PATENT NO. 6,404,476

Claim term	Acer's preliminary proposed construction	Extrinsic evidence
Wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes	The term "first electrode" means "an electrode strip formed on the first substrate for conducting electrical current" and the term "second electrode" means "an electrode strip contained in the circuit for supplying driving signals."	
Each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction	The term "first electrode" means "an electrode strip formed on the first substrate for conducting electrical current" and the term "second electrode" means "an electrode strip contained in the circuit for supplying driving signals."	

DATED: January 27, 2003

ALSCHULER GROSSMAN STEIN & KAHAN LLP

By _____
PETER J. WIED
Attorneys for Defendants
Acer Incorporated and Acer America Corporation

PROOF OF SERVICE

I am a resident of the State of California, over the age of eighteen years, and not a party to the within action. My business address is Alschuler Grossman Stein & Kahan LLP, The Water Garden, 1620 26th Street, Fourth Floor, North Tower, Santa Monica, California 90404-4060. On this 27th day of January, 2003, I served a true copy of the within documents:

ACER INCORPORATED AND ACER AMERICA CORPORATION'S PRELIMINARY PROPOSED CONSTRUCTIONS OF IDENTIFIED CLAIM TERMS

☑ by transmitting via facsimile the document(s) listed above to the fax number(s) set forth below on this date before 5:00 p.m.
The above transmission was reported as complete and without error. Attached hereto is a copy of the respective transmission report, which was properly issued by the transmitting facsimile machine.

☑ by placing the document(s) listed above in a sealed envelope with postage thereon fully prepaid, in the United States mail at Santa Monica, California, addressed as set forth below.

☐ by placing the document(s) listed above in a sealed envelope, with the overnight delivery charge prepaid, addressed as set forth below, and deposited in a box or facility regularly maintained by the overnight delivery service carrier, Federal Express.

☐ by personally delivering the document(s) listed above to the person(s) at the address(es) set forth below.

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I am readily familiar with the firm's practice of collection and processing correspondence for mailing. Under that practice it would be deposited with the U.S. Postal Service on that same day with postage thereon fully prepaid in the ordinary course of business. I am aware that on motion of the party served, service is presumed invalid if postal cancellation date or postage meter date is more than one day after date of deposit for mailing in affidavit.

I declare that I am employed in the office of a member of the bar of this court at whose direction the service was made.

I declare under penalty of perjury under the laws of the State of California that the above is true and correct.

Executed on this 27th day of January, 2003.

Jacqueline Spoonts

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Semiconductor Energy Laboratory Company, Ltd.

IN THE UNITED STATES DISTRICT COURT
FOR THE NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

SEMICONDUCTOR ENERGY LABORATORY COMPANY, LTD., Plaintiff, v. ACER INCORPORATED, ACER AMERICA CORPORATION, and AU OPTRONICS CORPORATION, Defendants.	CASE NO. C 02-02800 WHA SEL'S PROPOSED PRELIMINARY CLAIM CONSTRUCTIONS AND EXTRINSIC EVIDENCE

Pursuant to Patent L.R. 4-2, Semiconductor Energy Laboratory Company, Ltd. ("SEL") submits the following "Proposed Preliminary Claim Constructions and Extrinsic Evidence."

SEL's Proposed Preliminary Claim Constructions and Extrinsic Evidence are based upon information that is currently available to SEL. As additional information may become available through discovery and through disclosures pursuant to the Patent Local Rules,

SEL reserves the right to amend and supplement its Proposed Preliminary Claim Constructions and Extrinsic Evidence. SEL also reserves the right to amend and supplement its Proposed Preliminary Claim Constructions and Extrinsic Evidence once SEL has had an opportunity to review Acer Incorporated's, Acer America Corporation's and AU Optronics Corporation's Proposed Preliminary Claim Constructions and Extrinsic Evidence. SEL further reserves all objection to the use of this document or any of the information referenced herein in this case or in any other case or proceeding.

Pursuant to Patent Local Rule 4-2 and subject to the above limitations and reservations, SEL's Preliminary Claim Constructions and Extrinsic Evidence for the claim terms, phrases, or clauses that the parties have identified in their respective Proposed Terms and Claim Elements are as follows.

U.S. Patent No. 6,404,476

(1) The phrase "wherein said conductive adhesive extends lengthwise beyond each end of the first and second electrodes" should be construed to mean: wherein said conductive adhesive extends lengthwise beyond an end of the first electrode and an end of the second electrode. In addition to intrinsic evidence, SEL may rely on the testimony of Paul Kohl, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the prosecution history of the '476 patent and any related applications, and any references cited therein.

(2) The phrase "each end of said first electrode and said second electrode is completely covered by said resin in a lengthwise direction" should be construed to mean: an end of said first electrode and an end of said second electrode is completely covered by said resin in a lengthwise direction. In addition to intrinsic evidence, SEL may rely on the testimony of Paul Kohl, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the prosecution history of the '476 patent and any related applications, and any references cited therein.

U.S. Patent No. 6,355,941

(1) The phrase "non-single crystal semiconductor" (U.S. Patent No. 6,355,941) should be construed to mean: a semi-amorphous semiconductor, an amorphous semiconductor or a mixture thereof. In addition to intrinsic evidence, SEL may rely on testimony of Rafael Reif, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the prosecution history of the '941 patent and any related applications, and any references cited therein.

(2) The term "intrinsic" (U.S. Patent No. 6,355,941) should be construed to mean: not intentionally doped with an efficient dopant. In addition to intrinsic evidence, SEL may rely on testimony of Rafael Reif, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the prosecution history of the '941 patent and any related applications, and any references cited therein, and that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is supported by the extrinsic evidence, including the following references: Nakano, Shoichi, *et al.*, "High Performance a-Si Solar Cells and Narrow Bandgap Materials," Mat. Res. Soc. Symp. Proc. Vol. 49 (1985); Kaneko, S., *et al.*, "Amorphous Si:H Heterojunction Photodiode and its Application to a Compact Scanner," Mat. Res. Soc. Symp. Proc. Vol. 49 (1985); Suzuki, Kouji, *et al.*, "14.2/9:25 A.M.: High-Resolution Transparent-Type a-Si TFT LCDs," 146 SID 83 Digest (1983); Nagayasu, T., *et al.*, "1988 International Display Research Conference – A 14-in.-Diagonal Full-Color a-Si TFT LCD" (1988); Ichikawa, K., *et al.*, "14.1: 14.3-in.-Diagonal 16-Color TFT-LCD Panel Using a Si:H TFTs," 226 SID 89 Digest (1989); Martin, Russel A., *et al.*, "High Voltage Amorphous Silicon Thin-Film Transistors," IEEE Transactions on Electron Devices, Vol. 40, No. 3 (1993).

(3) The phrase "channel region (or channel forming region)" should be construed to mean: an area extending from the source to drain, including but not limited to, the channel. In addition to intrinsic evidence, SEL may rely on testimony of Rafael Reif, Ph.D., who will testify

that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the prosecution history of the '941 patent and any related applications, and any references cited therein.

U.S. Patent No. 6,404,480

(1) The phrase "second interlayer insulating film having at least two openings" (U.S. Patent No. 6,404,480) should be construed to mean: the second interlayer insulating film has at least two openings, as shown, for example in Figs. 1, 2A, 5F, 5G and 6-11 of the '480 patent. In addition to intrinsic evidence, SEL may rely on the testimony of Paul Kohl, Ph.D., who will testify that SEL's proposed claim construction, as viewed by one of ordinary skill in the art, is in accordance with the intrinsic evidence, including the prosecution history of the '480 patent and any related applications, and any references cited therein.

U.S. Patent No. 5,929,527

(1) The phrase "the film made of aluminum or a material containing aluminum as a principal component contains oxygen atoms at a concentration of $8x10^{18}$ atoms•cm^{-3} or less, carbon atoms at a concentration of $5x10^{18}$ atoms•cm^{-3} or less, and nitrogen atoms at a concentration of $7x10^{17}$ atoms•cm^{-3} or less" is readily understood and the terms therein should be accorded their plain meaning.

Date: January 27, 2003

Samuel B. Shepherd
Victoria F. Maroulis
QUINN EMANUEL URQUHART OLIVER & HEDGES, LLP

Jerold S. Solovy
Donald R. Harris
Stanley A. Schlitter
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MORI HAMADA & MATSUMOTO

By: _____
Attorney for Plaintiff SEMICONDUCTOR ENERGY LABORATORY COMPANY, LTD.

PROOF OF SERVICE

I, Joseph F. Marinelli, declare under penalty of perjury under the laws of the United States of America that the following is true and correct:

I am employed in the City of Chicago, in the County of Cook, State of Illinois, and an employee of Jenner & Block, LLC. I am a citizen of the United States, over the age of eighteen (18) years, and not a party to or interested in the within-entitled action. My business address is One IBM Plaza, Chicago, IL 60611.

I served the following document:

SEL'S PROPOSED PRELIMINARY CLAIM CONSTRUCTIONS AND EXTRINSIC EVIDENCE

I caused a true and correct copy of the above document to be served on the person listed below by the following means:

I enclosed true and correct copy of said document in an envelope and placed it for collection and mailing by Federal Express delivery on January 27, 2003, on the following party:

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I consigned true and correct copies of said document for facsimile transmission, and I enclosed true and correct copy of said document in an envelope and placed it for collection and mailing with the United States Post Office on January 27, 2003, on the following party:

Terrence D. Garnett
Alschuler Grossman Stein & Kahan LLP
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Facsimile No: (310) 907-2000

I am readily familiar with this firm's practice for collection and processing of documents for delivery in the manner indicated above, to wit, these documents were deposited for collection in the above-described manner.

Executed on January 27, 2003, at Chicago, Illinois.

Joseph F. Marinelli

HIGH PERFORMANCE a-Si SOLAR CELLS AND NARROW BANDGAP MATERIALS

SHOICHI NAKANO, YASUO KISHI*, MICHITOSHI OHNISHI, SHINYA TSUDA, HISASHI SHIBUYA*, NOBORU NAKAMURA, YOSHIHIRO HISHIKAWA, HISAKI TARUI, TSUYOSHI TAKAHAMA AND YUKINORI KUWANO

Research Center, SANYO Electric Co., Ltd.
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ABSTRACT

High performance a-Si solar cells were developed. A conversion efficiency of 11.5% was achieved for a textured TCO/p-SiC/in/Ag structure with a size of 1 cm^2 using the high quality i-layer fabricated by a new consecutive, separated reaction chamber apparatus. A conversion efficiency of 9.0% was obtained with a size of 10cm x 10cm. A high quality a-SiGe:H:F, which is a new narrow bandgap material for a-Si solar cells, was fabricated by a glow discharge decomposition of SiF_4 + GeF_4 + H_2.

A photo-CVD method was investigated in order to improve the interface properties of a-Si solar cells. A conversion efficiency of 11.0% was obtained with a solar cell in which the p-layer is fabricated by the photo-CVD method. a-SiGe:H films were fabricated by the photo-CVD method for the first time as a narrow bandgap material for multi-bandgap a-Si solar cells.

INTRODUCTION

Research and development of amorphous silicon (a-Si) materials are proceeding at a rapid rate. Their application to solar cells is also rapidly expanding. One of the main requirements for a-Si solar cells is to achieve higher conversion efficiency. Recently, their conversion efficiencies have been improved to a level of more than 11%[1] by improvements in a-Si materials and cell structures.

In this paper, first, we report an improvement of the conversion efficiency of a-Si solar cells by a new cell structure and high quality a-Si layers. Next, we discuss a-SiGe:H:F, which is a high quality new narrow bandgap material. Finally, we describe a-Si solar cells and a-SiGe:H films fabricated by a photo-CVD method, which is an attractive new method for fabricating a-Si materials.

HIGH PERFORMANCE a-Si SOLAR CELLS

Conversion efficiencies of a-Si solar cells have been increased owing to the development of new materials and new cell structures[2]. At present one of the key points for improving conversion efficiencies is the effective utilization of the wide spectrum of sunlight.

We achieved a conversion efficiency of 11.5% for a

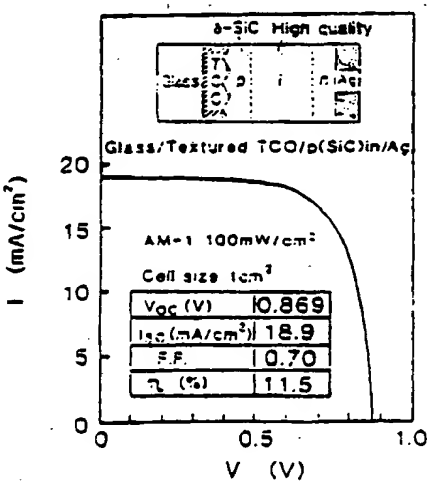

Fig. 1 Illuminated I-V characteristics of an a-Si solar cell

Mat. Res. Soc. Symp. Proc. Vol. 49. 1985 Materials Research Society

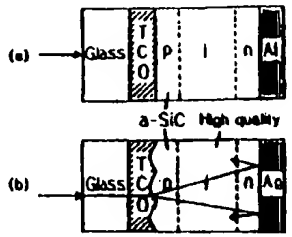

Fig. 2 Structures of a-Si solar cells
(a) Conventional structure
(b) New structure for high efficiency

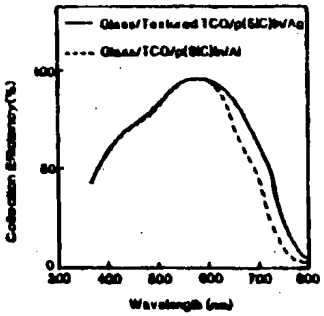

Fig. 3 Collection efficiency spectra of a-Si solar cells

textured TCO/p-SiC/in/Ag structure with a size of 4 cm^2 by improving the film quality of the i-layer (Fig. 1). The new cell structure is shown in Fig. 2 together with a conventional structure. A textured transparent electrode is employed at the front side of the cell and silver is used for the back electrode (Fig. 2(b)).

The textured transparent electrode reduces the reflection of the incident light at the front side of the cell. It also makes the light path in the i-layer longer by a scattering effect. Furthermore, the silver back electrode effectively reflects the long wavelength light which comes through the cell, and sends it back to the active region. Thus this new structure has an 'optical confinement effect' in particular for the long wavelength light. The quality of the i-layer is improved by reducing impurity concentrations and by optimizing fabrication conditions, in order to collect photo-generated carriers most efficiently.

Collection efficiency spectra of the cells are shown in Fig. 3. The collection efficiency in the long wavelength region is greatly improved by the optical confinement effect of the textured TCO and the silver back electrode.

A conversion efficiency of 9.0% was obtained for an integrated type a-Si solar cell submodule with a size of 10cm x 10cm.

PREPARATION AND PROPERTIES OF a-SiGe:H:F

In order to achieve much higher efficiencies, it is essential to develop high quality narrow optical bandgap (Eopt) materials. The optimum values of the Eopt are about 1.4eV to 1.5eV. Conventional a-SiGe:H films have been fabricated by a glow discharge decomposition of SiH_4 + GeH_4. However, their electrical and optical properties were not satisfactory.

Recently, Shimizu et al. have suggested a fabrication of hydrogenated fluorinated amorphous silicon germanium (a-SiGe:H:F) by a glow discharge decomposition of SiF_4 + GeF_4 + H_2[3]. In this paper we report a detailed investigation of the optimum fabrication conditions to form a-SiGe:H:F films for solar cells. Fabrication conditions were investigated in wide ranges in order to optimize the film properties.

a-SiGe:H:F films were fabricated with the apparatus and conditions shown in Fig. 4 and Table 1. The amounts of Si and Ge atoms were determined by ESCA. Fig. 5 shows variations of the properties of a-SiGe:H:F films as a function of the flow rate ratio of GeF_4 (R_{Ge}=GeF_4/(SiF_4 + GeF_4)). They show

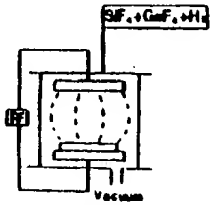

Fig. 4 Schematic diagram of the fabrication of a-SiGe:H:F

Table 1 Typical fabrication conditions for a-SiGe:H:F

Ts		150 ~ 250 °C
RF Power		20 ~ 100 W
Pressure		10 ~ 150 Pa
Flow rate (sccm)	SiF_4	20 ~ 150 sccm
	GeF_4	0.8 ~ 20 sccm
	H_2	10 ~ 200 sccm

good properties when R_{Ge} is less than 0.7%. When R_{Ge} is more than 0.7%, the dark conductivity(σd) becomes large and the value of $\sigma ph/\sigma d$ approaches unity.

Fig. 6 shows Raman spectra of (a) a film of R_{Ge}>0.7%, (b) a film of R_{Ge}<0.7% and (c) a conventional a-SiGe:H film. Spectrum (b) is almost the same as (c). However, spectrum (a) has only one peak at 305cm^{-1}, which originates from microcrystalline germanium (μc-Ge). Thus it was found that films of R_{Ge}>0.7% are μc-Ge rather than a-SiGe:H:F. Therefore, it is necessary to precisely control the flow rate of material gases.

Other fabrication conditions were investigated in order to attain higher film qualities. Fig. 7 shows properties of a-SiGe:H:F films as a function of the substrate temperature (T_s). It was found that excellent film properties were obtained when Ts is between 200°C and 250°C (σph = 3 x 10^{-4} Ω^{-1} cm^{-1}, σd = 1 x $10^{-7}\Omega^{-1}$ cm^{-1} when Eopt = 1.5 eV).

The Eopt and the Ge content (C_{Ge} = Ge/(Si + Ge)) are linearly related as follows:

Eopt = −0.8 x C_{Ge} + 1.75 ..... (1)

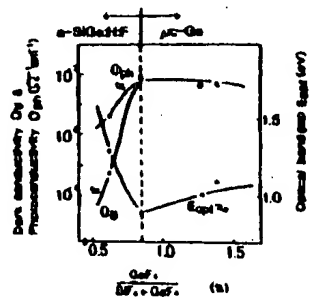

Fig. 5 Properties of a-SiGe:H:F films as a function of the gas flow rate ratio of GeF_4

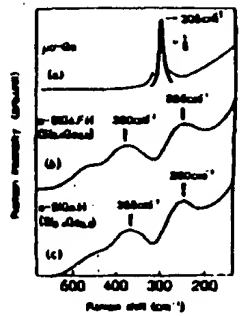

Fig. 6 Raman spectra of Si-Ge alloys
(a) Film of R_{Ge}>0.7%
(b) Film of R_{Ge}<0.7%
(c) Conventional a-SiGe:H (R_{Ge}=GeF_4 /(SiF_4 + GeF_4))

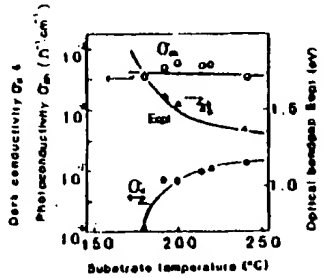

Fig. 7 Properties of a-SiGe:H:F films as a function of the substrate temperature

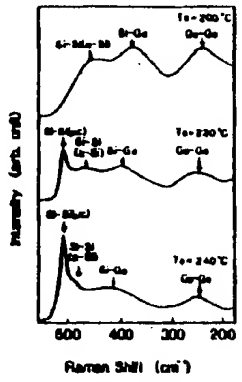

Fig. 8 Raman spectra of a-SiGe:H:F films as a function of the substrate temperature

This relation is qualitatively the same as that of conventional a-SiGe:H [6].

New structural information for a-SiGe:H:F films was obtained using Raman spectroscopy. Fig. 8 shows the Raman spectra of three a-SiGe:H:F films fabricated at different T_s. All the spectra show three broad peaks which originate from Si-Si bonds (480 cm^{-1}), Si-Ge bonds (400 cm^{-1}) and Ge-Ge bonds (250 cm^{-1}) in a-SiGe:H:F. In addition to these peaks, the spectra of the films of T_s = 220°C and T_s = 240°C show a narrow peak at 500 cm^{-1}, which originates from microcrystalline silicon. This result means that the silicon atoms in a-SiGe:H:F films partially microcrystallize when T_s is high, which suggests a wide-range controllability of film properties.

a-SiGe:H:F also shows excellent device properties. The I-V characteristics of Schottky diodes are shown in Fig. 9. A Schottky diode using a-SiGe:H:F has a rectification ratio of 10^7 at a bias of 1 volt, which is greater by 2 orders than that using a-SiGe:H.

As the a-SiGe:H:F films have excellent optical and electrical properties as well as excellent device properties, it is promised that high conversion efficiencies are obtained for solar cells using them.

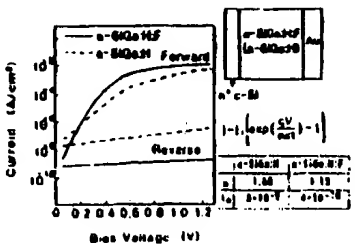

Fig. 9 I-V characteristics of Schottky diodes using a-SiGe:H:F and a-SiGe:H

Table II Typical reaction conditions of the photo-CVD method

Gas	Si_2H_6 C_2H_2 B_2H_6	Si_3H_8 $SiH_2(CH_3)_2$ Ge_2H_6
Total Flow Rate	10 - 100sccm	
Substrate Temp.	200 - 350°C	
Pressure	10 - 400Pa	

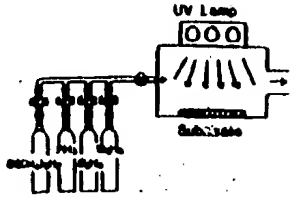

Fig. 10 Schematic diagram of the photo-CVD method

PROPERTIES OF a-Si ALLOYS AND SOLAR CELLS FABRICATED BY A PHOTO-CVD METHOD

A photo-CVD method, in which material gases are decomposed by ultraviolet rays, has recently attracted much attention as a new fabrication method[1]. The photo-CVD method is expected to form high quality interfaces because there is no damage to a-Si films caused by ion bombardment.

The schematic reaction apparatus and typical fabrication conditions of the photo-CVD method are shown in Fig. 10 and Table II. Low-pressure mercury lamps were used as a light source.

Fig. 11 shows SIMA depth profiles of In (Indium) atoms near the TCO/p and p/i interfaces of a-Si solar cells. When the p-layer is fabricated by the plasma CVD method, In atoms in the ITO layer diffuse into the p and i layers by ion bombardment during the fabrication process (broken line). When the p-layer is fabricated by the photo-CVD method, however, In atoms don't diffuse at all (solid line). The interface properties of a-Si solar cells fabricated by the photo-CVD method are excellent, thereby improving the collection efficiency in the short wavelength region. At present we have obtained a conversion efficiency of 11.0 % for an a-Si solar cell in which

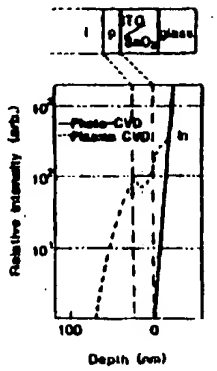

Fig. 11 SIMA depth profiles of In atoms in a-Si solar cells

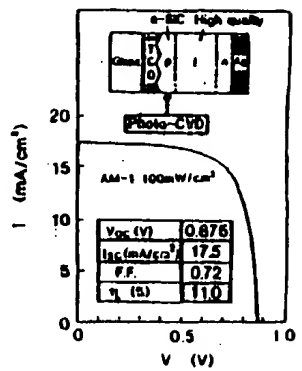

Fig. 12 Illuminated I-V characteristics of an a-Si solar cell using the photo-CVD method

the p-layer was fabricated by the photo-CVD method (Fig. 12). Higher conversion efficiencies are promised when the fabrication conditions are set to optimum values for the photo-CVD method.

Interface properties are especially important for multi-bandgap solar cells because they have a number of interfaces. Therefore, fabrication of a narrow bandgap material by the photo-CVD method is desirable for multi-bandgap solar cells. We have fabricated a-SiGe:H films by the photo-CVD method for the first time and controlled their Eopt. Si_2H_6 + GeH_4 + H_2 gases were used as material gases. The Eopt could be controlled between 1.7 eV and 1.05 eV by varying the flow rate ratio of material gases (Fig. 13). The Eopt and the Ge content are again linearly related by Eq.1.

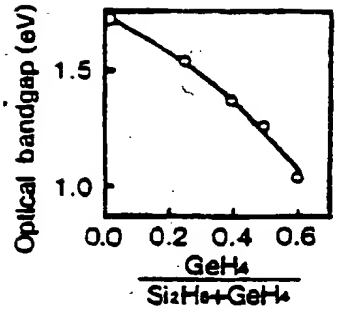

Fig. 13 Optical bandgaps of a-SiGe:H films fabricated by the photo-CVD method as a function of the flow rate ratio of material gases

Higher interface properties and higher conversion efficiencies are expected when this material is applied to solar cells.

CONCLUSION

Improvements in conversion efficiencies, new narrow bandgap materials, and improvements in interface properties by a photo-CVD method were discussed in view of their application to a-Si solar cells.

A conversion efficiency of 11.5% was achieved for a textured TCO/p-SiC/in/Ag structure with a size of 1 cm^2 by improving the film quality of the i-layer. A conversion efficiency of 9.0% was obtained for an integrated type a-Si solar cell submodule with a size of 10cm x 10cm.

a-SiGe:H:F films were fabricated from SiF_4 + GeF_4 + H_2 and excellent properties (σph = 3 x 10^{-4} Ω^{-1} cm^{-1}, σd = 1 x 10^{-7} Ω^{-1} cm^{-1} at Eopt = 1.5 eV) were obtained. Partially microcrystallized a-SiGe:H:F films were obtained.

A photo-CVD method was investigated in order to improve the interface properties of a-Si solar cells. A conversion efficiency of 11.0% was obtained for a solar cell in which the p-layer was fabricated by the photo-CVD method. Furthermore, high quality a-SiGe:H films were fabricated by the photo-CVD method for the first time as a new narrow bandgap material.

ACKNOWLEDGEMENT

This work was supported in part by NEDO as a part of the Sunshine Project under the Ministry of International Trade and Industry.

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AMORPHOUS Si:H HETEROJUNCTION PHOTODIODE AND ITS APPLICATION TO A COMPACT SCANNER

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ABSTRACT

This paper reports heterojunction photodiode properties and its application to a compact scanner. The photodiode has ITO / p-a-SiC:H / a-Si:H / metal structure. This diode has high photo to dark current ratio and small photocurrent saturation voltage, because of the excellent blocking characteristics for a heterojunction with large built in potential. Moreover, a-Si:H / metal contact has been investigated. A contact linear image sensor has been fabricated using the heterojunction photodiode array and compact optical system. Performance tests showed excellent results. Good reproduced images have been obtained.

INTRODUCTION

A contact linear image sensor has been developed to produce a compact facsimile or OCR (1)(2)(3). Conventional equipment uses a small size IC sensor and high magnification lens system, which requires about 200 mm optical path length to scan a document. On the other hand, a contact linear image sensor, whose width is the same as the document, does not require this high magnification lens system. Therefore, compact equipment can be built.

Hydrogenated amorphous silicon (a-Si:H) is suitable material for application to this long linear image sensor, because of its large area producibility, high photosensitivity and material stability. In this sensor, blocking structure photodiodes, such as Schottky barrier diode (3)(4), p-i-n diode (5) and MIS diode (6) have been employed in order to obtain small dark current and quick photoresponse. Among these blocking diodes, the Schottky barrier diode has the simplest structure to fabricate a photodiode array. However, Schottky barrier formation is sometimes unstable, due to surface plasma damage during indium tin oxide (ITO) sputtering deposition (7).

In order to obtain a stable and simple structure blocking diode, heterojunction photodiode, in which p type amorphous SiCx:H is inserted between undoped a-Si:H and ITO electrode, has been developed. This paper reports the heterojunction photodiode characteristics and its application to compact scanners.

DIODE STRUCTURE AND PREPARATION

Figure 1 shows elementary structure of the Schottky barrier diode and the heterojunction photodiode. In the Schottky barrier diode, undoped a-Si:H was produced by plasma deposition of SiH on a metal coated glass substrate. Then ITO was magnetron-sputtered. The undoped a-Si:H was 1-1.5 um thick. In the heterojunction diode, 300-400 A thick p-a-SiCx:H deposition followed the 1-1.5 um thick undoped a-Si:H deposition. The p-a-SiCx:H was produced by plasma deposition of SiH_4, CH_4 and B_2H_6 mixed gas.

Figure 2 shows optical gap energy and conductivity for undoped and boron doped a-SiCx:H. Increase in carbon concentration causes an increase in optical gap energy and a decrease in the film conductivity. The conductivity increases by boron duping. In the heterojunction diode, amorphous SiCx:H was produced by the CH_4 / SiH_4 + CH_4 = 0.5 gas mixture. This amorphous Si[illegible]

has the 1.97 eV optical gap and 10^{-8} S-cm dark conductivity. Activation energy, measured from temperature dependence of dark conductivity, was 0.4 eV.

DIODE CHARACTERISTICS

Figure 3 shows I-V characteristics in dark and lighted conditions for a Schottky barrier diode and a heterojunction diode. In both diodes, Cr metal was used for the lower electrode. The photocurrent shows 10^{-2} A/cm under 1501x T-6 LED light (570 nm peak intensity wavelength) illumination at -1 V reverse voltage. The photocurrent saturation, which is caused by unity collection efficiency for incident light, is observed at small voltage. In the heterojunction diode, the photocurrent saturates without any applied voltage. This small saturation voltage is due to high internal field at the heterojunction and gives small operation voltage for image sensors.

The darkcurrent for the Schottky barrier diode shows a relatively large value (10^{-11}-10^{-9} A/cm²) at -1V reverse voltage. On the other hand, the heterojunction diode exhibits very small dark reverse current (10^{-12}- 10^{-11} A/cm²) and a photo to dark current ratio as high as 10^4 has been obtained. This dark current keeps constant value up to 200°C thermal annealing in air, while dark current of the Schottky barrier diode is changed by this thermal annealing.

Figure 4 shows I-V characteristics for the heterojunction diode using various metals as lower electrodes. The reverse dark current shows almost the same value for the lower electrode material. It is different from the previously reported result, where the dark reverse current depends on the lower electrode material [3]. The forward current depends on the metal electrode material. Large forward current and good rectification have been obtained using low work function material except for Al.

Figure 5 shows an energy band diagram for the heterojunction diode without applied voltage. High built-in potential fully depletes the undoped a-Si:H layer. Photogenerated carrier drifts towards each electrode due to the high internal field in the undoped a-Si:H layer. Thus, photocurrent saturates without applied voltage. The small reverse current and stable characteristics for the heterojunction indicate that heterojunction does not suffer significant plasma damage during ITO sputtering and that the heterojunction is a good electron barrier. The dependence on the lower electrode material indicates that the reverse current is not hole injection current from the lower electrode, while forward current is mainly electron current flow through a-Si:H/metal contact. The temperature dependence of the I-V characteristics for diodes using Cr and Pd as lower-electrode was measured. Plots of $\ln(Js/T^2)$ vs $1/T$ are shown in fig 6, where Js is a forward current. These closely match the thermionic emission theory with barrier heights Φ_B of 0.9 eV for a Pd electrode and 0.72 eV for a Cr electrode. In fig 6, plots of $\ln(Js)$ vs $1/T$ are also shown, where Js is a reverse current. These give almost the same activation energy, 0.85 eV, and indicate that reverse current is mainly generation current.

Figure 7 shows spectral responses for the heterojunction diode and a homojunction diode using p-a-Si:H. The heterojunction diode has high sensitivity in the shorter wavelength due to light window effect of p-a-SiCx:H. Both diodes have high sensitivity for the LEDs used in the contact linear image sensor.

APPLICATION TO A COMPACT SCANNER

Figure 8 shows a contact linear image sensor exploded view. This sensor consists of LED arrays, a rod lens array and a long linear image sensor. LED arrays illuminates a document and reflected signal light is introduced

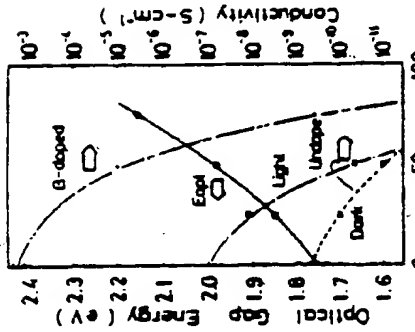

Fig. 2 Optical gap energy and conductivity for undoped and boron doped a-SiCx:H

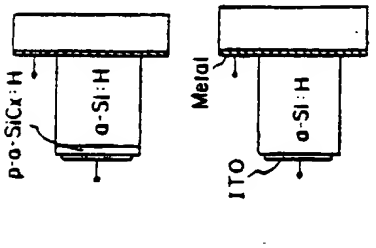

Fig. 1 Heterojunction diode and Schottky barrier diode structure

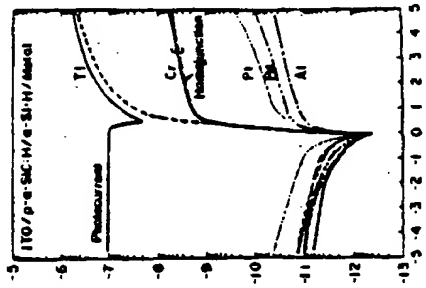

Fig. 4 I-V characteristics for heterojunction diode using various metals as lower electrode.

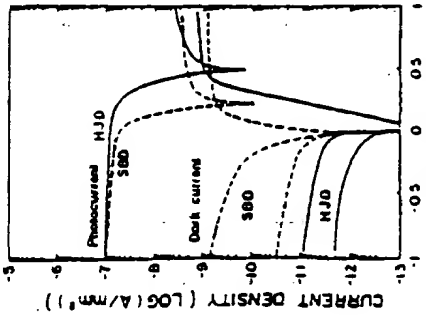

Fig. 3 I-V characteristics in dark and lighted conditions for heterojunction diode and Schottky barrier diode.

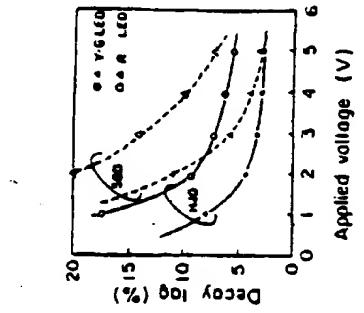

Fig. 10 Decay lag characteristics at first field

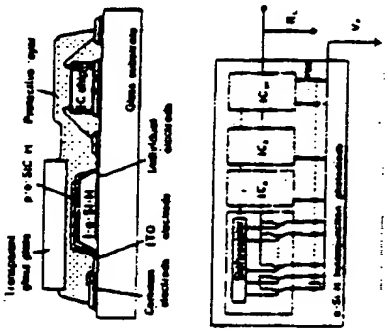

Fig. 9 Cross sectional view and driving circuit

Fig. 11 Contact linear image sensor and reproduced image

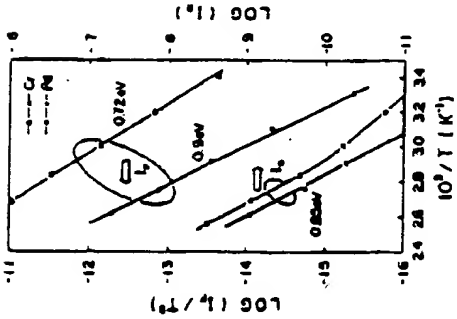

Fig. 6 Temperature dependence of forward current (I_F) and reverse current (I_R).

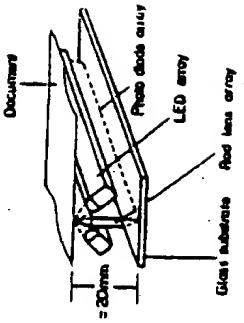

Fig. 8 Contact linear image sensor exploded view

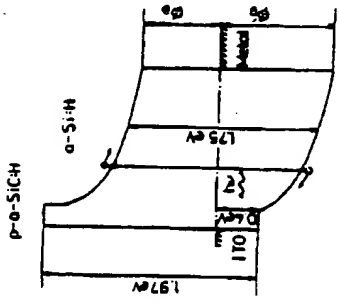

Fig. 5 Energy band diagram

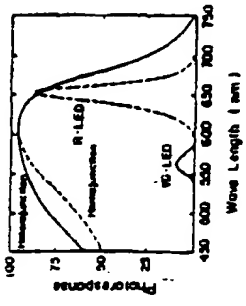

Fig. 7 Spectral response for heterojunction diode and homojunction diode. Light emission spectra for YG-LED and red LED are also shown.

to the linear image sensor through the rod lens array. Active length of the image sensor is 216 mm. The optical path between the document and the linear image sensor is 20-40 mm. Therefore, a compact scanner was achieved.

Figure 9 shows a cross sectional view and driving circuit for the linear image sensor. The linear image sensor has an 8 element /mm, 1728 element heterojunction diode array and driving ICs. Both were fabricated and mounted on a 230 x 30 mm^2 glass substrate. The driving IC consists of shift register and 64 MOS FET switches, which are connected to the associated heterojunction diode using wire bonding.

The image sensor is operated in the charge storage mode with 1 msec / line scanning speed. 30dB SN ratio has been obtained at 0.15 lx-sec exposure using Y-G LED. Figure 10 shows image lag characteristics for the image sensor. The image sensor using heterojunction diode has 1.5% decay lag for Y-G LED and 6 % decay lag for Red LED (650 nm peak intensity wave length) at -5 V applied voltage. The large decay lag for the Red LED is due to dispersive transport for hole. This decay lag is smaller than that of the image sensor using the Schottky barrier diode under this applied voltage.

Figure 11 shows the contact linear image sensor and a reproduced image printed by a thermal printer. This sensor is a compact scanner with 240 mm x 50 mm x 30 mm. Images were successfully reproduced with 8 lines / mm resolution.

CONCLUSION

A heterojunction photodiode, using p type a-SiCx:H has been investigated and applied to a compact scanner. The heterojunction is stable and has good electron barrier with high built in potential. It was also clarified that there is no hole injection at a-Si:H / metal contact. These result in high photo to dark current ratio for the photodiode and small operation voltage and good lag characteristics for the image sensor. A contact linear image sensor was fabricated. This sensor shows excellent performance. Good reproduced images have been obtained.

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14.2/9:25 A.M.: High-Resolution Transparent-Type a-Si TFT LCDs

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Introduction

LC-TV display panels using crystalline silicon substrates on which both MOS FET/capacitor arrays and gate-bus drivers are simultaneously integrated have already been reported[1)2)]. Although the active matrix shows high speed response, the displaying is restricted to the reflective mode. Also, the display area is limited by the available Si wafer size. Recently, it has been reported that an amorphous Si thin film transistor (a-Si TFT) is available for an active matrix circuit in a liquid crystal display (LCD) panel[3)]. The LCD with a-Si TFT appears to overcome the difficulties of the above two limitations. However, detailed performances of a-Si TFT LCD, such as dynamic characteristics, contrast or response time, have not been reported.

This report presents basic characteristics for the high resolution transparent a-Si TFT LCD panels which have been developed in our laboratory. The main features for the LCD panels are as follows: (1) display area; 44 x 60 mm, (2) pixels; 220 x 240, (3) pixel pitch; 200 x 250 μm, (4) LC materials; Nuesc-host (GH) LC for TV display and twisted-nematic (TN) LC for graphic display.

Device Structures

A cross section view of the LCD panel is shown in Fig. 1. The panel consists of a glass substrate with active matrix circuits, in which a-Si TFTs are used for controlling individual picture elements, a top glass substrate with counter ITO electrode and a LC layer. Each pixel includes one a-Si TFT and one storage capacitor. All of the processing stages to form matrix circuits on the glass substrate were carried out with conventional photolithographic techniques. 1000 Å thick Mo was used for gate electrodes and address bus lines. 1 μm thick Al was used for source and drain electrodes and data bus lines. Both electrodes in capacitors were constructed with ITO films. Both insulators for gate and for capacitor were prepared with the same CVD SiO_2 film. Undoped a-Si film and subsequent P-doped a-Si film were deposited by glow discharge technique. The channel length and width of the a-Si TFT were 10 μm and 140 μm, respectively. After circuits fabrication, the passivation layer, including a metal light shield layer, was applied to the a-Si TFT.

Static Characteristics of a-Si TFTs

Figure 2 shows channel current, I_D, versus gate voltage, V_G, characteristics for the a-Si TFT covered with the above mentioned passivation layer. These transfered characteristics correspond to a TFT whose dimensions are 10 μm channel length and 1500 μm channel width for drain voltages, V_D, of 5 and 10 V. The channel width of the TFT shown in Fig. 2 is about 10 times wider than that used in matrix circuits. The off-resistances of 1×10^{12} Ω and 3×10^{10} Ω are achieved for V_D of 5 and 10 V, respectively. On/off ratio is about 5×10^6 for 5 V V_D and about 3×10^5 for 10 V V_D. From the slope and the extrapolation on the linear region of the curve plotted in square root of I_D against V_G, field effect mobility, μ_n, and threshold voltage, V_{th}, can be estimated as 0.3 $cm^2/V.s$ and 5 V, respectively. As typical values, about 0.5 $cm^2/V.s$ for μ_n and 3 V for V_{th} were obtained. The I_D-V_D characteristics measurement with curve tracer showed good ohmic characteristics and small hysteresses loop. From these evidences, it is concluded that the a-Si TFTs well operated as field-effect-transistors.

Dynamic Characteristics of Elemental Circuit

A 60 pF external capacitor was connected to the source electrode of the a-Si TFT to investigate the circuit dynamic operation. Each storage capacitor in the matrix circuits was about 6 pF and the channel width of the a-Si TFT in the simulating circuit were about 10 times larger than that used in matrix circuits, so that the dynamic characteristics for the simulated circuits closely resembled those for actual matrix circuits. The measured wave forms are shown in Fig. 3. The upper trace represents a 20 V gate pulse, the middle trace represents a 10 V drain pulse and the lower trace represents the output voltage at the external capacitor. The repecition time is 100 msec. It can be seen that the drain potential is transfered within about 40 μsec, which enables displaying operation to follow the TV signals under a line at a time mode. The potential drop through the parasitic capacitor between gate and source electrode is about 1 V, which is smaller than the V_{th} value. For the holding performance, potential decay is only about 0.3 V during 100 ms. These dynamic characteristics indicate that the scanning ability corresponds to more than 400 lines/frame in 60 frames/s operation.

Display Characteristics

The LCD panels were fabricated with both GH and TN liquid crystals. The effective displaying area was about 54 % of the matrix element area. The LC layer thickness was about 10 μm. The LCD panel was driven by a line at a time method. The LC layer was driven to operate in the ac mode. The dependences of contrast ratio on bias voltage are shown in Fig. 4 for TN LCD and in Fig. 5 for GH LCD. In these experiments, bias voltages were applied in video rate, 60 μs/line and 60 frames/s. Half of each drain voltage was applied to the counter ITO electrode. The results indicate that entirely adequate operation can be established under 15 V V_G and 10 V V_D. This means that these LCD panels are fully driven by conventional CMOS ICs.

Figures 6 and 7 demonstrate TN-LC display and GH-LC display examples, respectively, with a fluorescent light source. The display quality was hardly affected by the incident light. Although a small decrease in contrast was observed, the LCD panel operated by scanning 511 lines/frame.

Conclusion

A 44 x 60 mm liquid crystal display, with high resolution, 20 pixels/mm^2, and high contrast, was established by a-Si TFT/capacitor matrix array. The minimum time needed to store 90 % of applied signal voltage into the storage capacitor through the on-state a-Si TFT was about 40 μsec under 15 V gate pulse and 10 V drain pulse bias conditions, which were fully supplied by the conventional CMOS ICs. Scanning ability for displaying was more than 400 lines/frame in 60 frames/s.

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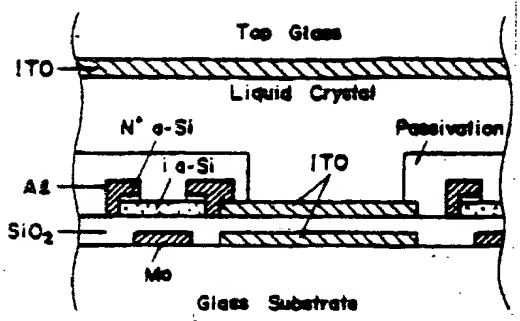

Fig.1 Cross sectional view of a-Si TFT/capacitor structure.

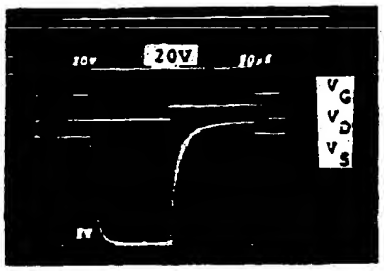

Fig.3 Pixel circuit dynamic characteristics.

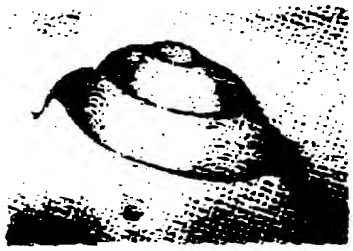

Fig.6 Photograph of TN-LC display.

Fig.7 Photograph of GH-LC display.

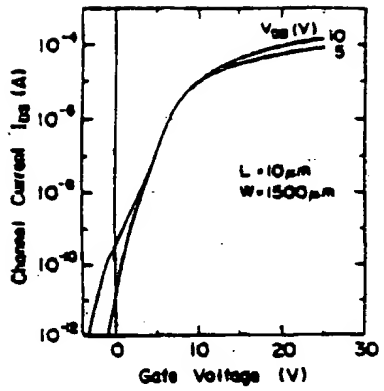

Fig.2 Transfered characteristics of a-Si TFT.

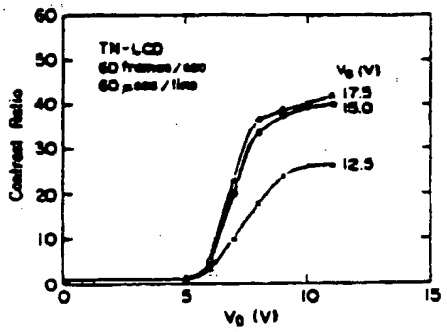

Fig.4 Contrast ratios of TN-LC display.

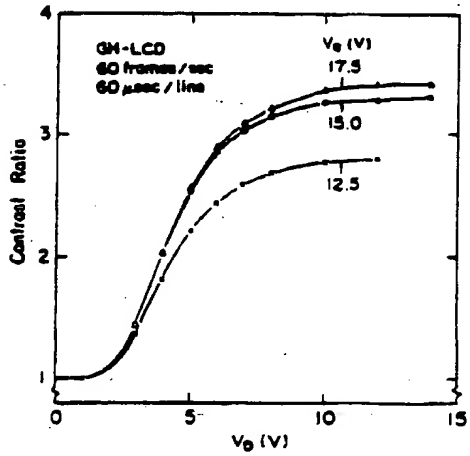

Fig.5 Contrast ratios of GH-LC display.

1988 INTERNATIONAL DISPLAY RESEARCH CONFERENCE

A 14-IN.-DIAGONAL FULL-COLOR a-Si TFT LCD

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Introduction

A 14-in.-diagonal full color a-Si TFT-LCD has been developed. The panel has 308,160(642H x 480V) pixels. The display provides excellent video pictures with good horizontal resolution(about 420 lines) and with high contrast ratio in a wide range of viewing angle. The contrast ratio is more than 100:1 at the optimum viewing angle and is more than 10:1 for the horizontal viewing angle of 120 degrees. The color pixels are arranged to form a triangular configuration. The color reproducibility of the display is equivalent to a CRT.

Recently, active matrix LCDs addressed by a-Si TFTs have been enthusiastically studied as the most promising candidates for applications like color TVs and portable computer displays. There have been many reports on progresses on size, resolution, and performance of the panels.[1] [2] [3] [4] But there seems to be few displays which provide good pictures uniformly in large area.

We have succeeded in the development of a large-area LCD with excellent performances. Several design features and the display performance of the present panel are described below.

TFT Structure

The TFT of the present panel has an inverted-staggered structure. Figure 1 shows a cross sectional view of the TFT. The W/L ratio of the TFT is 1.7. The TFT has a double-layered gate insulator which consists of TaOx and SiNx so as to reduce defects such as breakdowns or leakages between the metal layers. The ON/OFF current ratio is more than 10^7 under dark condition. Since the active matrix has no additional storage capacitor, geometrical values of the TFT are determined in consideration of off-state characteristics.

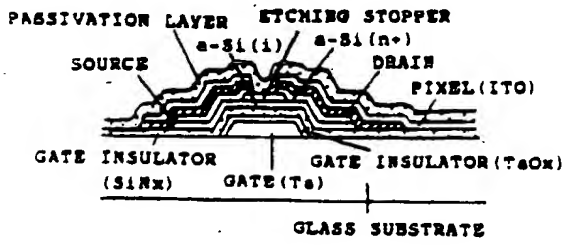

Figure 1 Schematic cross section of a-Si TFT

Pixel & TFT Arrangement

The triangular pixel arrangement is adopted to the present panel to obtain good color reproducibility.[5] A new design of TFT arrangement is also applied to the panel. A pixel is divided into four subpixels. Therefore, the panel has 1,232,640 subpixels. Each subpixel consists of a TFT and a transparent electrode and is placed at a point of intersection of separated gate and source bus lines as is shown in Figure 2. As a result, the triangular pixel arrangement is adopted to the present panel without bending any bus lines. In addition, if one of the TFTs driven by the same signal is damaged, it causes no entire pixel defect, but a subpixel defect which can hardly be noticed in moving pictures.

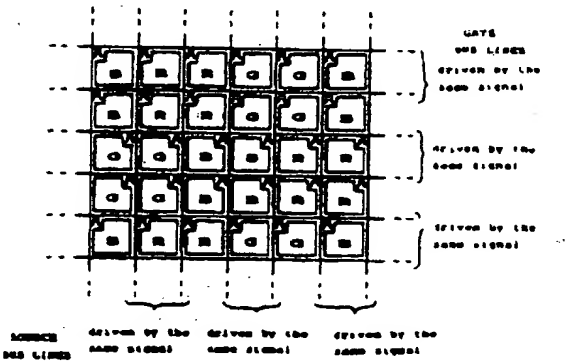

Figure 2 Schematic diagram of TFT arrangement

LC Panel Preparation

Materials for alignment layer and liquid crystal are optimized to obtain an excellent value of voltage storage ratio higher than 97% during an off-state. Polarizers are arranged to be "normally-white" configuration.

An interlaced scanning method is adopted. The present display is driven by the signal whose polarity is alternated in every scanning line so that a flickerless picture can be obtained.

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Display Performances

Figure 3 and Figure 4 show the transmittance-voltage curve and the viewing angle dependence of contrast ratio respectively. The contrast ratio of the present display is more than 100:1 at the optimum viewing angle. It is more than 10:1 for the horizontal viewing angle of 120 degees and for the vertical angle of 50 degrees. Figure 5 shows the color coordinates of the present display with a fluorescent backlight on the CIE chromaticity diagram. The color reproducibility is equivalent to a CRT. Specifications and performances of the present display are summerized in Table 1. The TV images on the present LCD are demonstrated in Figure 6, 7.

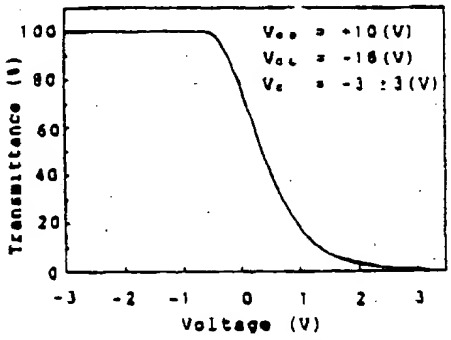

Figure 3 T-V curve

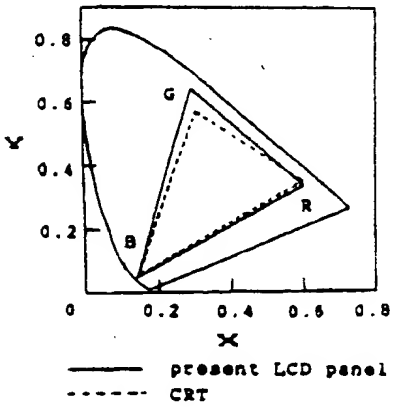

Figure 5 The color coordinates for the present LCD panel

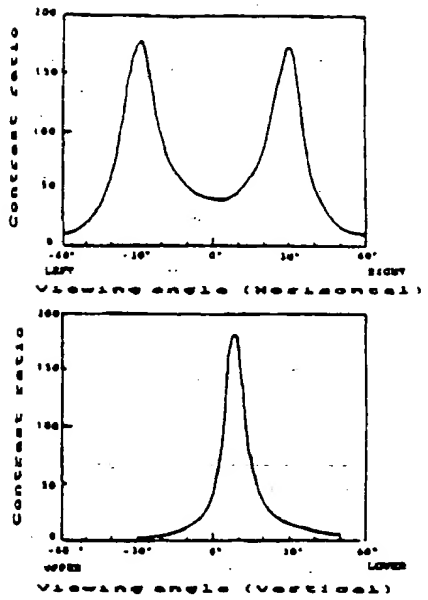

Figure 4 Viewing angle dependence of contrast ratio

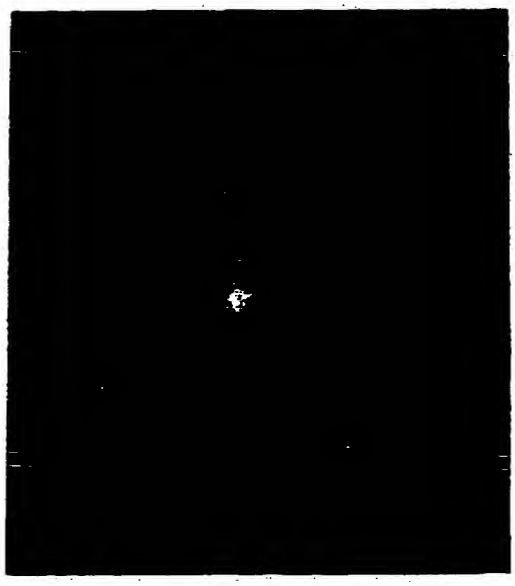

Figure 6 The photograph of the TV image on the present LCD

Table 1 Specifications and performances of the present LCD

Number of pixels		308,160 (642(H) x 480(V))
Number of TFTs		1,232,640 (1,284(H) x 960(V))
Pixel pitch (mm x mm)		0.41 (H) x 0.428(V)
Subpixel pitch (mm x mm)		0.205(H) x 0.214(V)
Screen size (mm x mm)		278(H) x 221(V) [14" diagonal]
Color pixel arrangement		triangular
LC mode		TN [normally white]
Maximum contrast ratio		>100:1
Viewing angle	Horizontal	120° (C.R. >10:1)
	Vertical	50° (C.R. >10:1)

Summary

A 14-in.-diagonal full color a-Si TFT-LCD has been developed by means of a new design of TFT arrangement and the optimizations of the factors which dominates off-state characteristics. The display has 308,160(642H x 480V) pixels (1,232,640 subpixels) and provides good pictures by its high contrast ratio(more than 100:1 at the optimum viewing angle).

A new design of TFT arrangement adopted to the present display realizes high display quality and leads to high production yield at the same time owing to triangular pixel arrangement with straight bus lines.

Acknowledgement

We would like to thank Mr. M. Miyuki, Mr. T. Kozu and Mr. M. Ishii for their encouragement and support. We also wish to express gratitude to the other members involved in this work.

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Figure 7
The photograph of the TV image on the present LCD

14.1: 14.3-in.-Diagonal 16-Color TFT-LCD Panel Using a Si:H TFTs

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INTRODUCTION

Recently, pocket TV's using TFT/LCD technology have come to be commercially available (Ref.1). Current displays range in size up to 5" diag. Larger display sizes are preferable, however, in the application to information display for computer peripherals. In addition to this, a larger number of dots is also required for such information displays. We have developed a 14.3" diagonal, 1440x1100 dots (1,584,000 dots total) TFT/LCD panel. A large screen size display with redundant TFT circuits has already been reported(Ref.2). The TFT/LCD panel presented here has no redundant TFT circuits. Simulation in the design phase of the TFT array and careful inspection in the fabrication process are the keys to the development of this TFT/LCD panel.

DESIGN

DOT ARRANGEMENT

The dots are quadruply arranged and one color pixel for color display is composed of red/green/blue/white dots. Thus, one color pixel can display 16 colors by combinations of on and off of each color dot. The present panel displays 720x550 pixels for color and 1440x1100 pixels for mono. The dot pitch is 200μm in both directions of x and y, and the display area size is 288mm x 220mm (14.3" diag.).

TFT STRUCTURE

The structure of TFT's is inverted-staggered, and there is no etch stopper for the n+ etching. The cross sectional view of the TFT/LCD is shown in Fig.1, and a microphotograph of the developed TFT is shown in Fig.2. The W/L of the TFT is 35/7μm. The storage capacitance, which is connected in parallel with the LC cell, is formed between the transparent display electrode of the nth gate line and the (n-1)th gate line. Therefore, the thickness of the insulator for the storage capacitor is same as that for the TFT gate insulator, and the storage capacitor can be formed without any additional mask or process.

TFT ARRAY

For a TFT/LCD panel, a larger aperture ratio, or transmission factor, for each dot is desirable. Therefore, the width of the gate line should be decreased as much as possible. On the other hand, there is a limitation in the thickness of the gate line, because thick gate line will cause line openings at the crossover. This means that a narrow gate line can result in high gate line resistance and in a long delay of the gate pulse at the far end of a line. Thus, there is a trade-off between the gate line resistance and the aperture ratio of a dot. Driving from both ends of a gate line is one of the solutions to this problem. However, this is not economical, because twice as many gate driver IC's would be needed. The 14.3" diagonal TFT/LCD panel presented here was designed with the aim of driving the gate lines from one end. The use of low resistance Mo/Ta alloy as gate metal is the key to achieving this goal (Ref.3). The required width of the gate line, and thus the aperture ratio of a dot, was determined from a simulation of the gate pulse delay as follows.

The gate pulse width, tg, is 14.5μsec when the panel is driven at a frame frequency of 62.5Hz. The gate pulse delay, which is a function of gate line resistance and gate line capacitance, was designed to be less than half of tg. In this case, the gate line width was designed to be 70μm. Thus, the aperture ratio of ITO electrode is 46%.

There are constrictions at the crossovers of gate and data lines which have the effect of reducing the capacitance on the gate lines but increasing their resistance. Therefore, there is an optimum gate line width at the crossover. This width was determined from a simulation of the gate pulse delay. From the simplified simulation, the gate line resistance is calculated as follows:

$$R_g = \frac{\rho}{d_g}\left(\frac{L_c}{W_c} \cdot \frac{P_x - L_c}{W_g}\right) M_x$$

where, ρ is the resistivity of Mo/Ta thin film; dg is the gate line thickness; Lc and Wc are the length and width of the constriction, respectively; Wg is the width of the gate line; Px and Mx are the pitch of dots and the number of dots in the horizontal direction, respectively. The gate line capacitance is

$$C_g = \left(\frac{\varepsilon_{GI}}{T_{GI}}(S_c + S_T + S_{CS}) + \frac{\varepsilon_{LC}}{d_{LC}} S_0\right) M_x$$

where, ε_{GI} and ε_{LC} are the dielectric constant of the gate insulator and liquid crystal, respectively; Tox and d_{LC} are the thickness of the gate insulator and liquid crystal layer, respectively; Sc, St, Scs and S_0 are the area of the constriction, the drain-gate overlap, storage capacitance and the gate line exposed to LC layer, respectively. The gate pulse delay is τ=Rg·Cg, and the condition which minimize the gate pulse delay is

$$\frac{\partial \tau}{\partial W_c} = 0$$

Therefore, the gate line width at the crossover is

$$W_c = \sqrt{\frac{L_c\left(\varepsilon_{LC}(P_x - L_c)W_g^2/d_{LC} + \varepsilon_{GI}(S_T + S_{CS})/T_{GI} + \varepsilon_{LC}S_0/d_{LC}\right)W_g}{\left(\varepsilon_{GI}W_g/T_{GI} + \varepsilon_{LC}(L_c - W_g)/d_{LC}\right)(P_x - L_c)}}$$

When Wg=70μm, the Wc is calculated to be 36μm in the present design.

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LIQUID CRYSTAL CELL

Many factors, such as contrast ratio, viewing angle dependency, response time and color change will affect the legibility. Unfortunately, the optimum values for the design parameters are different for each factor. In usual, the LC cell gap, dd , or retardation, Δnd is determined to maximize the contrast ratio. For a large size display, however, the uniformity of the background color with respect to viewing direction is very important in normally black mode. The background color depends upon the LC cell gap. It depends as well on viewing direction(Fig.3). Therefore, for the developed panel, the LC cell gap was so chosen that the background color was not greatly changed by a change in the viewing direction. Such selection of LC cell gap is also good for the gap tolerance.

FABRICATION PROCESS

The gate line material is prepared by the DC magnetron sputtering using Mo/Ta alloy target. The resistivity of sputtered Mo/Ta thin film is 45μohm-cm. Fig.4 shows the SEM image of the cross sectional view of a sputtered Mo/Ta gate line. The columnar structure is seen. The tapered etching of gate lines is important for avoiding data line (Mo/Al) openings. The angle of taper is 10 degrees as shown in Fig.4(a), achieved by a dry etching process. After etching, the Mo/Ta gate line was anodized. Fig.4(b) shows the cross sectional view of the gate line after anodic oxidation. A sharp interface edge is formed between the anodized and the metal layer, and no columnar structure is seen in the anodized layer. The thickness of Mo/Ta alloy decreases 20% by the anodic oxidation, and the total gate line thickness is increased 33%. Anodized oxide film forms a part of the gate insulator of the TFT and is effective for the reduction of inter-layer shorts (Ref.4). Thus, three layers (TaOx/SiOx/SiNx) in all make up the gate insulator. After the anodic oxidation, four layers, SiOx/SiNx/i a-Si:H/n+ a-SiiN layers, were continuously deposited by multi-chamber plasma-CVD. After forming the drain and source electrode, the n+ layer was etched off using a dry etcher. A SiOx/SiNx double layer is used for the TFT passivation layer. The increase of Vth after passivation is smaller for this double layer in comparison to the SiNx single layer as passivation.

As mentioned before, the LC cell gap is so designed that the background color is not changed greatly by the viewing angle. This also means that the present design is good for the gap tolerance and the spacer density can be reduced. In order to fix the cell gap precisely (±0.1μm), a large number of spacers, such as 100/mm², are usually distributed. In the developed panel, however, 20/mm² is enough for the fixing of the cell gap. Moreover, there are following advantages of
(1) less light leakage
(2) less liquid crystal degradation
(3) decrease in damage to TFT and color filter.

The good retention of the charge on the cell capacitance during the TFT-off period is the key to achieve a high quality LCD panel. The retention is greatly affected by the cleanliness during the LC cell fabrication. More than 90% retention was achieved by paying close attention to the elimination of contaminants.

The driver IC's are connected to the TFT array circuits using TAB technology. The outer lead of the TAB is tin-plated. An anisotropic conductive film of thermosetting type is used for the connection between glass substrate and TAB.

TFT AND DISPLAY PERFORMANCE

Fig.5 shows the typical Id-Vg characteristics of the TFT. The threshold voltage and mobility are 4V and 0.5cm²/V·sec, respectively. Fig.6 shows the brightness vs. signal voltage characteristics of the panel. The brightness vs. signal voltage characteristics are not changed much by a change in the gate pulse width from 9 to 56.4μs. This indicates, on average, the liquid crystal is charged up sufficiently during the period of the gate pulse width of 14.5μs. The brightness of the panel is 100nit. The viewing angle for vertical and horizontal directions are 30degree(upper)/20degree(lower) and >40degree(right/left), respectively. At the designed Δnd value, the comparison in the optical characteristics with those of the conventional design leads to the following results:
(1) The decrease in the contrast ratio in the normal direction is less than 25%, and this decrease is scarcely perceived by the human eyes.
(2) The horizontal viewing cone is comparable. The vertical viewing cone is slightly narrower.

Fig.7 shows one of the display images on the developed TFT/LCD panels. The specifications of the panel are summarized in Table1.

CONCLUSION

A 14.3" color TFT/LCD with 720x550 pixels and 1440x1100 pixels for mono have been developed for information display applications. The panel was fabricated without any circuit redundancy in the TFT array. We have thus shown the possibility of the fabrication of defect free, 14" TFT/LCD panels. This results from the insulator structure which reduces the inter-layer shorts and from careful process and inspection throughout the fabrication.

ACKNOWLEDGMENT

The authors would thank to Dr.W.E.Howard of IBM Yorktown Research, Mr.S.Hirano of IBM Yamato Lab., Mr.S.Sano of Toshiba R&D Center and Dr.T.Shimada of Toshiba Elec.Dev.Eng.Lab. for encouragement and helpful discussion to this work.

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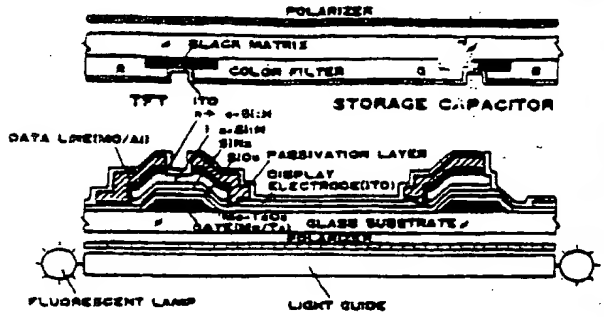

Fig.1 CROSS SECTIONAL VIEW OF TFT/LCD

Fig.2 MICROPHOTOGRAPH OF TFT ARRAY

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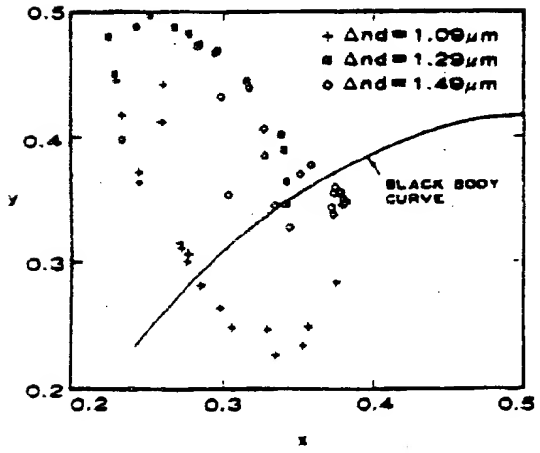

Fig.3 BACKGROUND COLOR CHANGE DUE TO CHANGE IN Δnd

Fig.4 CROSS SECTIONAL VIEW OF TAPER-ETCHED Mo/Ta

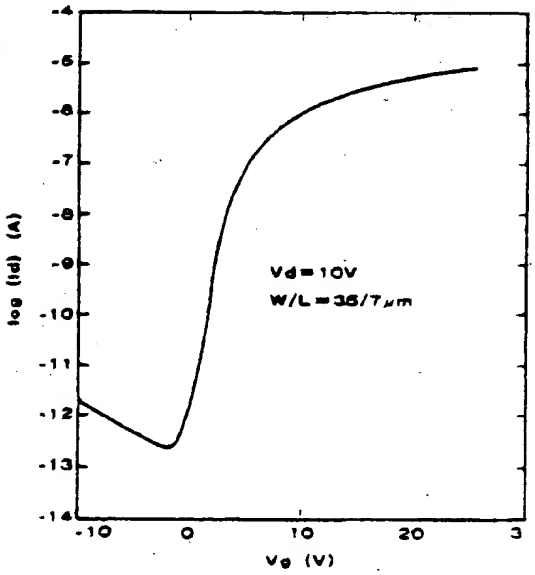

Fig.5 Id-Vd CHARACTERISTICS OF TFT

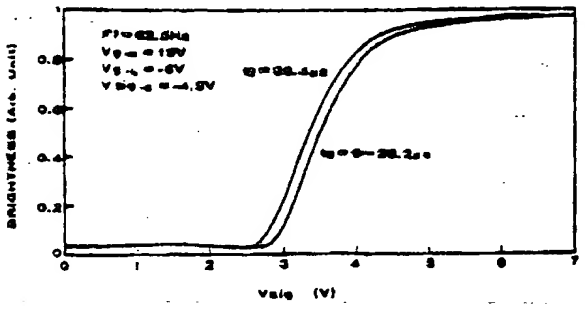

Fig.6 BRIGHTNESS-DATA LINE VOLTAGE CHARACTERISTICS

TABLE I SPECIFICATIONS OF THE 14.3" COLOR TFT/LCD

NUMBER OF DOTS	:	1440 x 1100
NUMBER OF PIXELS	:	720 x 550
DISPLAY AREA SIZE	:	288mm x 220mm
DOT PITCH	:	200um x 200um
COLOR ARRANGEMENT	:	QUADRUPLE, R/G/B/W
BRIGHTNESS	:	100nit
CONTRAST RATIO	:	30
VIEWING ANGLE	:	±40degree (HORIZONTAL) +30degree (UPPER) -20degree (LOWER)

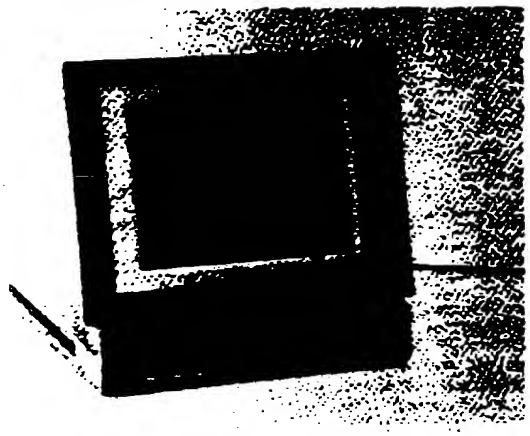

Fig.7 DISPLAY IMAGE OF THE 14.3" COLOR TFT/LCD

*Source of the image:K.Matakenaka and K.Kito, "Selected Graphic Design",Gakusyu Kenkyusya 1985.

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High-Voltage Amorphous Silicon Thin-Film Transistors

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Abstract—High-voltage MOSFET's have been fabricated in a large-area thin-film amorphous silicon technology. The transistors have an offset gate structure which allows them to operate at in excess of 400 V. Basic fabrication steps and structure are discussed. These transistors have a gate-controlled region in series with an offset region where the current is space-charge-limited. The I_D-V_D characteristics exhibit a unique instability under drain voltage stress; there is a parallel shift in the I_D versus V_D characteristic to a higher V_D. This instability arises from the creation of localized states in the a-Si during depletion. It is analyzed through experiment and two-dimensional simulation. Structural variations are described, including the application of a field plate, to stabilize transistor drive current. Reliability and process uniformity are discussed for arrays of transistors. An appropriate circuit simulation model is discussed. Operation of output drive circuits with HVTFT's is shown, and the application of these to an electrographic plotter is described.

I. Introduction

RECENTLY amorphous silicon, a-Si, technology has found numerous applications because of its low cost and compatibility with low-temperature glass substrates [1], [2]. Circuits are fabricated with linear dimensions in excess of 30 cm. Thin-film transistors, TFT's, are widely used as pixel addressing elements in large-area flat-panel displays. They are also used in printing and scanning bars [3]–[5]. Many applications, however, require drive voltages well in excess of 100 V, for example, certain ferroelectric liquid crystals, electrophoretic or PLZT electrooptic displays, and electrographic plotters. For these applications a high-voltage TFT, HVTFT, is needed. This paper describes the fabrication, structure, and performance of a-Si HVTFT's and their application to electrographic plotters.

II. Process and Structure

Fig. 1 shows a cross section of an HVTFT and a low-voltage TFT, LVTFT. The HVTFT can be thought of as an accumulation-mode MOSFET with an offset drain. The offset prevents an excess field from breaking down the amorphous silicon nitride gate insulator. Because of its low conductivity, the intrinsic a-Si has low off current, although it is slightly n-type. The gated region controls the current flow in the same way as in an LVTFT.

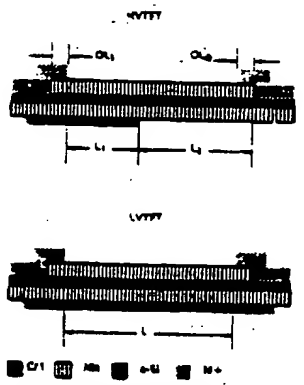

Fig. 1. Cross sections of a high-voltage thin-film transistor and a low-voltage thin-film transistor.

The fabrication process for the HVTFT is identical to that for the inverted staggered structure LVTFT. The substrate is 7059 borosilicate glass. To form the gates, a 50-nm chrome film is sputtered and patterned with wet etching. The gate silicon nitride, intrinsic a-Si, and passivation silicon nitride are deposited by plasma-enhanced chemical vapor deposition, PECVD, without removing the substrate from the system. The gate nitride is 300 nm thick. The intrinsic a-Si is 50 nm thick. The top layer of nitride, used as an etch stop and for surface passivation, is 150 nm thick. The top nitride is patterned to delineate the silicon island of the transistor by plasma etching. The vias to the gate chrome are etched, followed by depositions of N^+, phosphorus-doped, a-Si, 200 nm thick and a second layer of chrome. The second chrome and the N^+ a-Si become the source and drains of the HVTFT. They are patterned with the etch stopping on either bottom nitride, top nitride, or gate chrome. An intermetal dielectric of polyimide is deposited and patterned, followed by the sputtering and patterning of aluminum for interconnection. The final passivation is polyimide.

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The a-Si layer can be divided into several regions. On the source side the contact injects electrons into the channel. The source overlaps the top nitride just enough to prevent underlap. This is the region of length OL_S. The gate extends a distance L_1 beyond the end of the source overlap. On the drain side of the gate is the region of length L_1, known as the offset region.[1] The offset region extends to the drain contact. At the drain overlap OL_D, the current flows to the top interface and then out the drain contact.

III. Device Operation

a-Si HVTFT's have some properties in common with a-Si low-voltage TFT's and others in common with crystal silicon HV MOSFET's. They are, however, unique and some of their characteristics are very surprising [6]–[8].

When one examines the I_D versus V_D characteristics of the HVTFT, as in Fig. 2, the first striking point is the low drive current. This is due to the FET mobility being approximately 1 $cm^2/V \cdot s$. This is the same situation as with low-voltage a-Si TFT's. HVTFT's are still, nevertheless, very useful. Because of the insulating substrate material, parasitic capacitance is low, thus circuit speed is increased. Moreover, in many applications a large number of operations are done in parallel, raising the system speed.

Another significant point is the lack of avalanche multiplication. Because of the large amount of scattering, which causes the low μ_{FET}, there is no significant carrier multiplication, therefore dielectric breakdown or heating become the failure mechanisms at high voltages, rather than avalanche breakdown.

These HVTFT's can withstand very large drain voltages without increased leakage. Fig. 3 shows the subthreshold characteristics of an HVTFT. There is almost no difference between the leakage current at V_D = 40 V and V_D = 400 V. As with crystal silicon high-voltage transistors, the high-voltage operation is due to the drain voltage being dropped across the offset region.

As with other a-Si TFT's the threshold voltage and FET mobility are a strong function of CVD conditions. V_{Th} is typically between 1 and 2 V. The initial threshold is determined in large measure by the quality of the CVD of gate nitride and intrinsic a-Si. For example, contamination of these materials with oxygen will raise the threshold [9]. As with LVTFT's, the threshold shifts under gate bias [10]. Fig. 4 shows the threshold as a function of time for an HVTFT. V_{Th} is determined at a fixed current. The stress is a 50% duty cycle square wave with the HVTFT in a lightly loaded inverter with the supply at 400 V. The voltage of the square wave is 20 V. The shifts are due to creation of metastable states and relax back when in the unstressed state. The metastable states are due to dangling bonds in the a-Si network. They are created or destroyed by the movement of hydrogen in response to the position of the Fermi level in the a-Si. They are equivalent to those seen in low-voltage a-Si TFT's.

The source and drain overlaps, shown in Fig. 1, influence the transistor operation by influencing saturation current and shortening the effective offset region length, respectively. Together with the bottom gate, the source overlap determines the drive current. Because the drain overlap is at the drain potential, it pulls the current flow in the intrinsic a-Si to the top interface. In this way the drain overlap somewhat reduces the effective L_1. These effects have been discussed in detail elsewhere for low-voltage TFT's (Hack and Shaw [11]).

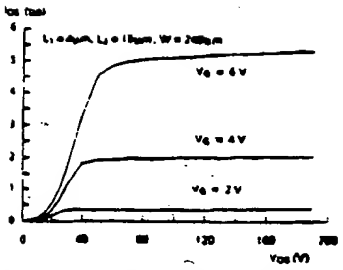

Fig. 2. Drain current versus drain-to-source voltage for a high-voltage thin-film transistor with gate-to-source voltage as a parameter.

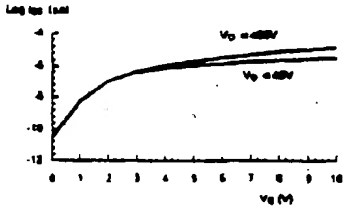

Fig. 3. Drain current versus gate-to-source voltage for a high-voltage thin-film transistor with drain-to-source voltage as a parameter.

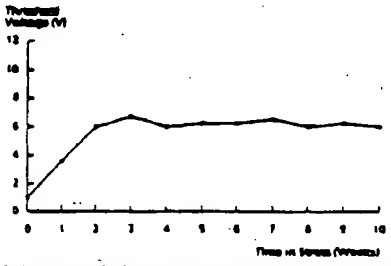

Fig. 4. High-voltage thin-film transistor threshold as a function of time in 50% duty cycle stress with the gate at 1 or 20 V and the drain loaded by a 700-kΩ resistor to 400 V.

[1] This has been referred to as the "dead region" in several previous publications. For clarity it is only referred to as the offset region in this work.

If improperly designed, a-Si HVTFT's show an unusual instability. The drain voltage for the onset of the rise in drain current can shift to higher voltages [6]. This arises from the creation of metastable states in the a-Si in the offset region near the gate edge [12]. Fig. 5 shows I_D versus V_D. Initially, the characteristics show a power law rise at low V_D (space-charge-limited current) [13], saturating at higher V_D (curve A). If the transistor is exposed to a high drain voltage stress with V_{GS} held below threshold, the characteristics shift along the V_D axis to higher voltages (curve B).

The instability can be well quantified by defining a quantity, called V_s, which measures the onset of injection of current into the offset region. An extrapolation of I_D versus V_D at the inflection point to zero current gives the value of V_s, as shown in Fig. 5. The result is only a weak function of gate voltage, but for this work it is measured at approximately V_{Th} + 5 V.

Changes in V_s are repeatable and saturate with time. This is shown in Fig. 6. As the stress is shifted from a high stress state, high V_D, and low V_G, to one of low stress with low V_D and high V_G, V_s falls with a time constant of minutes. These measurements are taken by applying dc biases for 3 min and then changing V_D and V_G for 3 s to measure V_s. This is done in a lightly loaded inverter circuit in which V_{out} is nearly equal to V_s. The measurement does not influence the results as shown by the lack of influence of the spacing between measurements on the results. If left in an unpowered state V_s drops back towards its original value.

It is important to remember the difference between shifts in V_s and shifts in V_{Th}. An increase in V_{Th} results in lower effective gate voltage, which will result in a lower saturation current for the same gate bias. An increase in V_s results in lower effective drain-to-source voltage, meaning that the onset of conduction occurs at a higher drain bias, yet the saturation current will not change. Since the equilibration effects responsible for both instabilities occur in different areas of the intrinsic a-Si, the instabilities are independent of each other and can therefore both be present, depending only on the type of stresses applied to the HVTFT. Like V_{Th}, however, a high level of V_s can be reset to a low value by an anneal of 200°C for 30 min.

The changes in V_s depend on the values of V_D and V_G such that the saturation value of V_s after a long stress is lowest at values of V_G near V_{Th}. Fig. 7 shows a plot of this effect. V_s (after a long stress) versus V_G is plotted for a lightly loaded inverter. The supply voltage is 400 V. The transistors has L_1 = 5 μm and L_2 = 25 μm. There is a large rise at negative V_G and a small rise at positive V_G (where current is flowing).

The V_s performance of HVTFT's is influenced by CVD in the same way that other device parameters, such as V_{Th} and μ_{FET} [9]. The initial value of V_s can be degraded by the addition of oxygen to the gate nitride and intrinsic a-Si. Likewise, V_s is also degraded by excessive deposition temperature and other factors influencing the LVTFT performance.

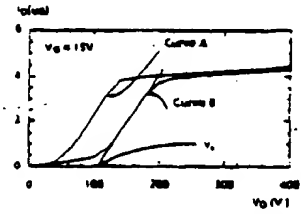

Fig. 5. I_D versus V_D for a high-voltage thin-film transistor. Curve A is the initial value after fabrication. Curve B shows the effect of stress with the channel off and the drain at high potential. The extrapolation from the inflection point of the curve gives the value of V_s.

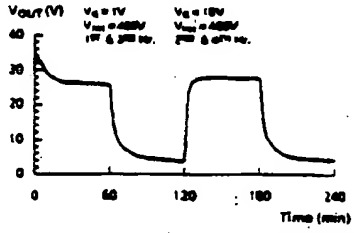

Fig. 6. The output voltage of an inverter made up of a high-voltage thin-film transistor and a 700-MΩ resistor to 400 V. Between measurements the transistor is off for the first and third hour and on for the second and fourth.

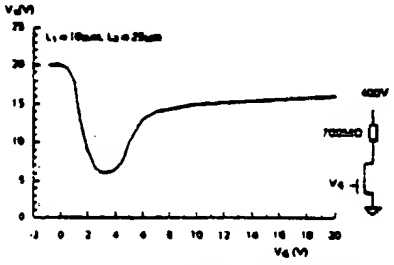

Fig. 7. The limiting value of V_s with time as a function of the gate voltage in stress using the inverter pictured. The minimum is near the threshold voltage of the transistor.

Finally, V_s is also not a problem of variable-source resistance. It is not effected by contact quality nor does the functional dependence agree with a source resistance.

IV. Origin of V_s

In the previous section most of the experimental data on V_s shifts have been presented. The origin of V_s has been inferred from these data and the nature of intrinsic a-Si. In this section, the nature of changes in V_s are described. In the following sections, an analytical model of the HVTFT and numerical simulations will be used to further elucidate the device physics of these transistors.

As stated earlier, the shifts in V_s arise from changes in

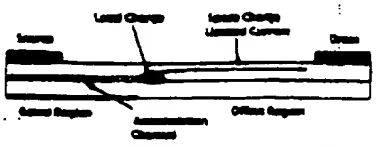

Fig. 8. A schematic cross section of a high-voltage thin-film transistor showing the location of localized charge that causes the V_t shift.

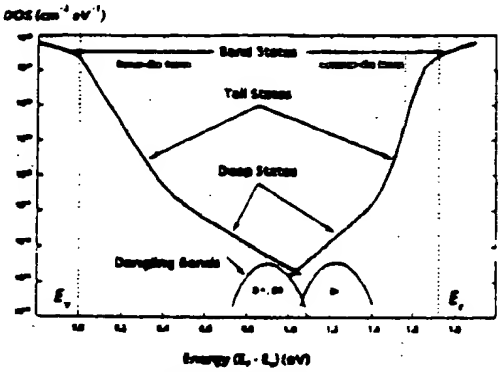

Fig. 9. Density of states for a-Si versus energy, showing the levels due to dangling bonds.

the density of states in the intrinsic a-Si in the offset region near the gate edge. Fig. 8 shows a schematic cross section of the transistor indicating the location of the region with the altered density which affects the conduction.

In its initial state, the HVTFT has a uniform density of states throughout the intrinsic a-Si. When a positive potential is applied to the drain, current flows. If the drain bias is below the saturation voltage, the current in the offset region is space-charge-limited, that is, it is not charge-neutral. The potential through the offset region rises nonlinearly. When the lateral field at the edge of the gate rises to a high enough level, the gated region saturates in the same fashion as with a low-voltage TFT. The only difference being that the intrinsic a-Si at the end of the gate acts as an effective drain.

With the transistor turned off (V_g below threshold) and the drain at high voltage, the offset region is depleted of carriers to below the intrinsic level at the drain and just above the edge of the gate. The high field due to the drain and due to the sharp corner of the gate (where the potential is held low) causes this depletion. When this occurs the amorphous silicon equilibrates to compensate. Dangling bonds and hydrogen rearrange to create more states, attempting to pin the Fermi level in the middle of the gap. This equilibration is similar to the more familiar equilibration seen when the a-Si is accumulated (the origin of positive V_{Th} shifts in LVTFT's).

Fig. 9 shows the density of states. The change in the density of states produces extra traps above the Fermi level, the D^+ levels, while the D^0 and D^- traps are reduced. These fill and this localized charge forms a "barrier" which the electrons must overcome before being injected into the offset region. In this "barrier" the field from the localized charge opposes the injection of charge. Because the drain is offset, the voltage applied to the drain contact does not all appear at the edge of the gate, but is dropped across that region more or less uniformly. This means that for a longer L_1 the same amount of charge near the gate edge will have more effect on V_t. If the field from the localized charge is E_{local} then a simple approximation to the change in V_t is

$$E_{local} L_1 = \Delta V_t$$

This can be thought of as an analogy to a lever arm. Although charge at any point in the offset region will influence the current flow, it has the most effect at the gate edge.

V. Analytical Theory

In modeling semiconductor devices one can use two complementary approaches. First is a full numerical solution of the transport equations which yields important information as to the device operating physics. Second is a simple semi-analytic model based on the appropriate device physics which can be used as a quick design tool to predict output characteristics.

The simple semi-analytic model for the high-voltage TFT is based on the physics derived from our comprehensive two-dimensional simulations, such that the overall device of length L is treated as being composed of two regions: the gated region, from the source electrode to the edge of the gate electrode, length L_1, which behaves as a conventional amorphous silicon transistor [14] of gate length L_1; and the offset region, which extends from the edge of the gate electrode to the drain. As undoped amorphous silicon is highly resistive, the current flow in region 2 is, in general, space-charge limited allowing for much higher current flow than would be obtained from ohmic conduction. Current continuity is maintained in both regions by the electric field in the channel (in the source-drain direction) at the interface of the gated and ungated regions (edge of the gate) which controls the injection of charge into the second ungated region. It is the effect of this boundary field that allows the high drain voltage to be safely dropped across the ungated region without causing high gate-to-channel potentials. At any given gate voltage (above threshold) as the drain potential is increased from zero, current flow is at first limited by the space-charge-limited flow in the ungated region. As the drain potential is increased further then the gated region, which acts like a conventional low-voltage TFT, approaches saturation and consequently the channel electric field near to the edge of the gated region increases. This high field, at the interface of the gated and ungated regions, prevents the injection of charge from the channel into the ungated region. Therefore, as the drain voltage

becomes even higher, the electric field at the interface increases preventing further injection of charge into the ungated region causing the device to saturate.

To derive the overall device current–voltage characteristics the TFT, in the gated region, or accumulation channel, the channel electric field F is related to the current flowing through it by the gradual channel approximation. For simplicity we neglect the dependence of the field-effect mobility, μ_{FET}, on gate voltage. Hence, as described in detail in [15], the free electron surface charge per unit area qn_s is related to the total charge induced into the channel Q_{ind} by

$$\mu_{FET}/\mu = qn_s/Q_{ind} \tag{1}$$

where μ is the electron band mobility. Following the gradual channel approximation for the gated region defining the source at $x = 0$ and the end of the channel at $x = L_1$, the total charge induced along the channel is related to the gate-to-source voltage V_{gs} and the threshold voltage V_{Th} by

$$Q_{ind} = C(V_{gs} - V_{Th} - V) \tag{2}$$

where V is the channel potential and C the gate capacitance per unit area. For an element of channel of length dx and width W the current I is given by

$$I = qn_s\mu W\, dV/dx = \mu_{FET}C(V_{gs} - V_{Th} - V)W\, dV/dx. \tag{3}$$

Integrating (3) from the source at $x = 0$ to $x = X$ and in potential from $V = 0$ at the source to $V = V(X)$ gives

$$IX = W\mu_{FET}C(V_{gs}V - V^2/2) \tag{4}$$

where $V_{gs} = V_{gs} - V_{Th}$.

From (4) it can be seen that when $X = L_1$ and $V = V_{gs}$ the current in the gated region saturates due to pinch-off at the end of the gated region, and its value I_{sat} is given by

$$I_{sat} = \mu_{FET}CWV_{gs}^2/2L_1. \tag{5}$$

Solving (4) for potential we obtain

$$V = V_{gs} - (V_{gs}^2 - 2XI/W\mu_{FET}C)^{1/2}. \tag{6}$$

The field in the channel parallel to the semiconductor–insulator interface at the boundary of the gated and ungated regions F_g is found by substituting for V from (6) and putting $X = L_1$ into (3).

$$F_g = IV_{gs}/(2L_1I_{sat}[1 - I/I_{sat}]^{1/2}). \tag{7}$$

From (7) it can be seen that as I approaches I_{sat} then F_g tends to infinity. This is important as when F_g is large it limits the injection of charge from this accumulation or gated region into the dead region. Thus as will now be shown, the overall transistor current cannot exceed I_{sat} because when I approaches I_{sat}, F_g becomes large preventing further charge injection into the ungated region. Once the channel is nearly saturated any increased drain voltage is dropped across this ungated region.

The voltage drop across the accumulation channel V_1 for a current I is given by

$$V_1 = V_{gs} - [V_{gs}^2 - (2IL_1/CW\mu_{FET})]^{1/2}. \tag{8}$$

To determine the current–voltage characteristics of the ungated region for the case of space-charge-limited current flow, Poisson's equation must be solved along the amorphous silicon for the edge of the gate electrode to the drain contact, with the starting boundary condition being the electric field calculated from the edge of the gated region. Owing to the relatively large density of states in the mobility gap of amorphous silicon the space charge is primarily determined by trapped charge n_t, whereas its conductance is determined by the number of mobile electrons n.

For a deep localized state distribution $g(E)$, varying exponentially with energy, having a characteristic temperature T_0, such that

$$g(E) = g_c \exp[(E - E_c)/kT_0] \tag{9}$$

where g_c is the density of deep states extrapolated to the conduction band edge, then when the injected charge density is much greater than the equilibrium charge density, n and n_t are given by

$$n = N_c \exp[(E_f - E_c)/kT] \tag{10}$$

where N_c is the effective density of states. Assuming zero-temperature statistics

$$n_t = g(E)\, dE = kT_0 \exp[(E_f - E_c)/kT_0] \tag{11}$$

and hence n and n_t are related by

$$n = N_c[qn_t/g_ckT_0]^\alpha \tag{12}$$

where $\alpha = T_0/T$. Thus solving Poisson's equation along the ungated region

$$dF/dx = qn_t/\epsilon = (kT_0/\epsilon)g_c[n/N_c]^{1/\alpha}. \tag{13}$$

Integrating (13) with the boundary condition $F = F_g$ at the start of the ungated region and noting that the current density $j = nq\mu F$ where μ is the electron band mobility gives

$$F^{(\alpha+1)/\alpha} = x[(1 + \alpha)/\alpha]\,(kT_0/\epsilon) \cdot g_c[j/q\mu N_c]^{1/\alpha} + F_g^{(\alpha+1)/\alpha}. \tag{14}$$

To obtain the potential drop across the ungated region V_2 for a current $I = jWt$, where t the thickness of the active layer, (14) is integrated with respect to x, yielding

$$V_2 = (1/K\beta)[(KL_2 + H)^\beta - H^\beta] \tag{15}$$

where $K = (1 + \alpha)(g_ckT_0/\alpha\epsilon)[I/q\mu N_cWt]^{1/\alpha}$ and

$$H = F_g^{(\alpha+1)/\alpha}$$

and

$$\beta = (1 + 2\alpha)/(1 + \alpha).$$

If the length of the ungated region L_2 is too long for current flow to be space-charge-limited (i.e., its ohmic

Fig. 10. Theoretical and experimental I_D–V_D characteristics for an L_1 = 20 μm high-voltage thin-film transistor.

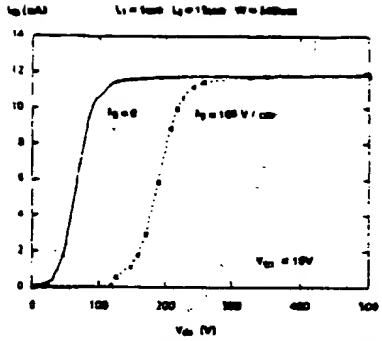

Fig. 11. I_D–V_D characteristics for an L_1 = 5 μm, L_2 = 15 μm high-voltage thin-film transistor, showing how an added boundary field will raise V_t.

resistance is lower than that determined by space-charge conduction at a given applied bias) then V_2 will simply be given by $V_2 = IR_2$ where R_2 is the resistance of the ungated region.

This one-dimensional model assumes that the ungated region is a parallel-plate structure. In practice, this region is much longer between its ends than it is thick, i.e., $L_2 >> t$. In order to apply this one-dimensional model to the real two-dimensional situation we have to include a large fringing capacitance between the source and drain accounting for the electric field stream lines. Hence we have introduced a correction factor into (15) such that the permittivity of the silicon ϵ has been multiplied by L/t [16].

In summary, to derive the overall current–voltage characteristics of the transistor:

1) Specify a current, I, ensuring that $I < I_{sat}$.
2) Calculate V_1 (voltage drop across gated region) from (8).
3) Calculate the boundary field connecting the gated and ungated regions using (7).
4) Calculate V_2 from (15).
5) Determine the overall voltage drop across transistor $V = V_1 + V_2$.

In Fig. 10 we show both the experimental and theoretical source–drain current–voltage characteristics for a high-voltage TFT with an L_1 = 4 μm and L_2 = 16 μm. In applying the model outlined in (1)–(15) we have used the following parameters: μ = 10 cm^2/V · s, gate overlap L_1 = 4 μm, μ_{FET} = 0.5 cm^2/V · s, g_c = 1.3 × 10^{18} cm^{-3} · eV^{-1}, T_0 = 1500 K, C = 1.34 × 10^{-8} F/cm^2, N_t = 10^{19} cm^{-3}, W = 240 μm, and t = 0.1 μm. From Fig. 10 it can be seen that our analytic model is in good agreement with the experimental data.

This semi-analytic model is also extremely useful in helping us to understand the V_t shift in these devices. This occurs when the region of amorphous silicon in the ungated portion of the device near to the edge of the gate becomes depleted (or in some cases accumulated) of electrons and extra defects are created in the a-Si in this region. These extra defects cause an additional "barrier" to the injection of charge from the gated to ungated regions. In our simple analytic model this has been represented by increasing the boundary electric field F_B to simulate the effects of this additional "barrier." In Fig. 11 we show the results of our analytic model for the normal case of no V_t shift, e.g., as shown in Fig. 10, and also a case where the boundary field has been increased by 10^3 V/cm at every value of V_{ds}. The results give an extremely good representation of an approximate 130-V V_t shift as experimentally observed.

VI. Numerical Simulations

In order to more fully understand the performance of HVTFT's we have used two-dimensional (2D) simulations to analyze its performance. We have utilized MANIFEST [17], a 2D finite-elements semiconductor device simulator. Because there are few holes in the semiconductor they have virtually no effect on the devices performance. Therefore, the solution is only for the potential and for the free and trapped electron concentration. The trapped electrons are accounted for by determining the proportion of trapped electrons to the total, based upon steady-state results.

Solutions for the potential and electron concentration throughout the intrinsic a-Si are determined. A transistor with L_1 = 15 and L_2 = 15 is chosen for the simulations because it could operate at V_D = 400 V. The doping simulates an N$^+$ contact on top of a 60-nm intrinsic layer. The gate dielectric is 300 nm thick. Overlap of the source and drain contacts are not simulated in this work, but their effect is well understood from previous work [11].

Fig. 12 shows the potential profile with the drain at 400 V and the gate at 0 V. Here current flow is very low. The voltage drop is nearly linear across the offset region except that the field is higher near the gate edge and near the drain. It is clearly seen that the drain potential is primarily dropped across the offset region. The voltage at the drain side of the gated region is very low. This is in the same fashion as with crystal silicon transistors in

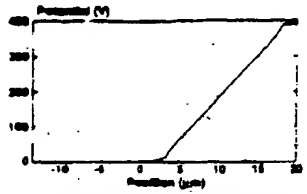

Fig. 12. Potential (at the bottom interface of the intrinsic a-Si) versus horizontal position for a standard HVTFT. The drain is from $X = 18$ to 20 μm. The source is from $X = -14$ to -12 μm. The gate is from -14 to 3 μm. The drain potential is 400 V and the gate is at 0 V.

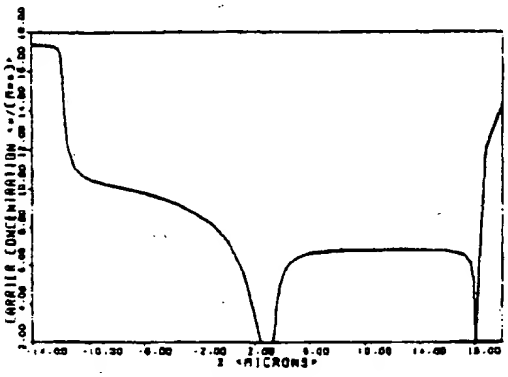

Fig. 13. Electron concentration (at the bottom interface of the intrinsic a-Si) versus horizontal position for a standard HVTFT. The drain is from $X = 18$ to 20 μm. The source is from $X = -14$ to -12 μm. The gate is from -14 to 3 μm. The drain potential is 400 V and the gate is at 0 V.

which the drain voltage is dropped across the lightly doped drain extension. In this case, however, the point of the offset region is only to reduce the voltage across the gate insulator. Because there is no significant avalanche multiplication there is no need to reduce the drain field.

As has already been discussed, the origin of the rise in V_t is the creation of local states due to shifts in the density of states caused by depletion of the intrinsic a-Si when the device is turned off. This depletion can be seen in a simulation of the electron density at the lower side of the TFT's intrinsic a-Si layer, Fig. 13. Notice that the density is lower at the gate edge. The depletion is greatest along the bottom surface of the intrinsic a-Si where the gate edge has the most influence. Although depletion may occur at the drain end, as well as near the gate, it will have little effect on V_t because it is so close that the drain field will easily overcome the induced "barrier."

Simulations in which the density of states is locally raised at the edge of the gate (to simulate the affect of depletion on the a-Si) show a V_t increase over that seen without the higher density of states [12]. This lends further credence to the explanation of the origin of V_t shifts.

VII. Structural Variations and Design Issues

To design optimally stable HVTFT's the values of L_1 and L_2 must be properly determined [6]. The a-Si HVTFT is not susceptible to avalanche breakdown, but the offset regions length is still important for device operation. First, it must be long enough to sufficiently drop the maximum drain voltage so as to prevent breakdown of the gate insulation. It also must be long enough that the depletion of the a-Si is not excessive; that would cause a buildup of charge and a rise in V_t. These issues point to a long L_2. On the other hand, as L_2 shortens the space-charge-limited current will rise more steeply with V_D. This means the initial value of V_t will be lower and that improves the HVTFT's overall performance. There is another beneficial effect to shorter L_2; because the field from the drain is stronger any built-up charge is more easily overcome. So short L_2 causes more charge buildup, but the initial value of V_t is lower and the charge is more easily overcome. For 400-V operation the optimum L_2 is in the neighborhood of 20 μm.

L_1 also influences V_t; it does so because for longer L_1 the edge of the gate is farther from the source overlap where the channel potential is held very low. A large extension of the gate allows a reduction in the field at the edge and thereby a reduction in the depletion of the a-Si. When L_1 becomes very long there is a reduction in the drive current. For the case of 400-V operation a value of $L_1 = 15$ μm has been found suitable; for longer values there is little effect on V_t.

Optimum design may therefore be considered to be the longest L_1 without lowering I_D and shortest L_2 without causing drain breakdown or excessive V_t due to extra depletion. This can yield HVTFT's whose V_t does not exceed 30 V under any operating condition.

VIII. Field Plates

Although HVTFT's have been optimized by adjusting L_2 and L_1 to have small variations in V_t there is still some room for improvement. This improvement is achieved by the addition of a field plate at positive potential. The field plate is located above the intrinsic a-Si layer covering the edge of the gate and part of the offset region. With this addition V_t is reduced to very low levels thus providing a very low on-voltage for inverters, in the neighborhood of 5 V for a 400-V inverter.

The structure of an HVTFT with a field plate [18] is shown in Fig. 14. The basic design is similar to that of the conventional HVTFT. L_1 and L_2 are defined in the same way and remain of similar lengths for the field-plated design. The field plate is described by its extension towards the source from the gate edge F_1 and by its extension over the offset region from the gate edge F_2. The material between the a-Si and the metal field plate is the passivation nitride, 150 nm thick, and 1 μm of polyimide. This serves to prevent insulator breakdown to the intrinsic a-Si layer. The length F_1 is determined by the alignment tolerance of the process. That region is needed to insure

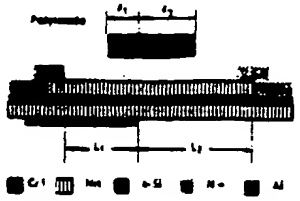

Fig. 14. Cross section of an HVTFT with a field plate.

that the edge of the gate is always covered by the field plate.

Because the field-plate insulator is much thicker than the gate insulator, there is less coupling of the potential from the field plate to the intrinsic a-Si layer above the gate. The potential of the silicon at the edges of the field-plated region is strongly influenced by the gate or drain electrodes potential. The desirable potential for the field plate can be determined simply by taking a transfer curve for an inverter controlled by the field plate. With a resistive load on the HVTFT, connected to an appropriate supply voltage, the gate is kept on and the voltage of the field plate is swept. The operating point is a voltage somewhat above the value at which the output of the inverter has fallen to its desired low value. For 400-V operation with $L_1 = 25$ μm and $F_2 = 13$ μm an operating voltage above 50 V is desired.

Fig. 15 shows how much the field plate improves the performance of the HVTFT. These improvements in the on-voltage can be thought of as having two origins, both arising from the weak accumulation of the intrinsic a-Si caused by the field plate's potential. First, the weak accumulation of the a-Si effectively shortens the offset region, but, importantly, without greatly raising the maximum gate field with the drain high. This effectively shorter L_1 causes the drain current to rise faster with increasing V_D. Thereby the initial value of V_x is lowered. This effectively shorter L_1 has another effect. Because the drain potential is somewhat more closely coupled to the potential in the intrinsic a-Si at the edge of the gate, charge there will have less effect than without the field plate. This means that for a given amount of increased charge due to changes in the density of states from depletion there will be less change in V_x. The combination gives overall lower V_x, both initially and after a stress. So we see that the field plates effect can be thought of as increasing the rate of rise of drain current with drain voltage and increasing the effectiveness of drain voltage in overcoming the "barrier" caused by excess charge in the offset region.

The operation of the field plate can be better understood through use of 2D simulations. We have modeled an HVTFT with $L_1 = 15$ μm, $L_2 = 15$ μm, $F_1 = 2$ μm, $F_2 = 6$ μm, and a field-plate insulator of 1 μm, and all other parameters the same as in the previous simulations. Fig. 16 compares the potential in the intrinsic a-Si layer with the gate at 0 V, the drain at 400 V, and the field plate at 100 V to the potential without a field plate. One can see

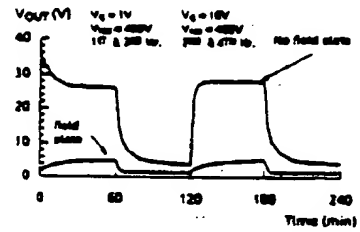

Fig. 15. The output voltages of inverters made up of a high-voltage thin-film transistor and a 700-MΩ resistor to 400 V. Between measurements the transistor is off for the first and third hour and on for the second and fourth. Transistor with and without field plates are used. The field plate potential is 100 V.

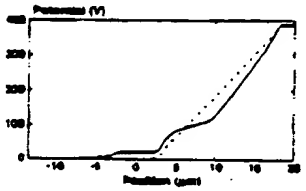

Fig. 16. Potential (at the bottom interface of the intrinsic a-Si) versus horizontal position for an HVTFT with a field plate (solid line) and without (dashed line). The drain is from $X = 18$ to 20 μm. The source is from $X = -14$ to -12 μm. The gate is from -14 to 3 μm. The field plate is from $X = 1$ to 9 μm. The drain potential is 400 V, the gate is at 0 V, and the field plate is at 100 V.

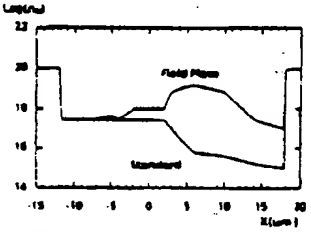

Fig. 17. Electron concentration (at the top interface of the intrinsic a-Si) versus horizontal position for HVTFT's with and without field plates. The drain is from $X = 18$ to 20 μm. The source is from $X = -14$ to -12 μm. The gate is from -14 to 3 μm. The field plate is from 1 to 9 μm. The drain potential is 35 V and the gate is at 5 V. The field plate is at 50 V.

that the field plate raises the electrostatic potential near the gate end of the offset region, but does not pin the potential there. This is due to the relative thickness of the gate insulator being smaller by a factor of three. In this way L_1 is effectively shortened, as described above.

The field is still dropped across the offset region and the gate insulator does not see a particularly high field. There is, however, more depletion at the gate side (bottom) of the intrinsic a-Si from the field plate, raising the field at the gate end of the offset region. This will create more localized charge, however, the field plate raises the electron concentration along the top interface by several orders of magnitude. In Fig. 17 the electron concentration

at the top of the intrinsic a-Si layer is plotted versus horizontal position for the field-plated and standard HVTFT with V_G = 5 V, V_D = 35 V, and V_{FP} = 50 V. This top surface region of extra conductivity and the enhanced field allows the field-plated transistor to easily overcome the extra charge "barrier."

IX. Application to Electrographic Plotting

The HVTFT fabrication process is completely compatible with the standard low-voltage TFT process. This makes possible the simple multiplexed high-voltage inverter circuit shown in Fig. 18. The pullup resistor is an integrated, phosphorus-doped, a-Si layer, fabricated in the same deposition as the n^+ source/drain contact. Low voltage TFT (Q_L) is used as a pass transistor to selectively charge or discharge the gate capacitance of Q_H. The multiplexing scheme works by enabling a group of adjacent drivers with a single word line (V_G). Each bit of data (V_1 to V_n) is presented to the drain of each Q_L in the group, so that when the word line is enabled the bit is written to the HVTFT gate. The gate capacitance of the HVTFT is on the order of 2 pF and the hold times of these drivers easily achieve 100 ms, due to the very low leakages of the LVTFT's. For applications in wide electrographic plotters, this multiplexing scheme can be a used to switch a large number of drivers in a one-dimensional array. We have built a 12-in-wide integrated electrographic print array encompassing 4736 high-voltage drivers, at a 400-drivers/in pitch.

To ensure print uniformity, the output voltage of the inverter in the output low state must not vary more than 15 V across the array and must pull down to voltages of 20 V or less. These points bring up a number of design considerations unique to a-Si circuits involving HVTFT's. One of which is that due to equilibration effects, the generation of traps below mid-gap cause the ON-state threshold of an a-Si device to shift to higher voltages with use. This problem can be overcome by sufficiently high value of pullup resistor (500–1000 MΩ), and high drive voltages (20–25 V). This ensures that the thresholds of the HVTFT's can shift at different rates for different areas of the writing head and still achieve uniform print density over the life of the head.

With the above choice of operating voltages, however, the HVTFT is susceptible to V_t shifts. As already discussed, gate-to-source voltages applied to the HVTFT that are well below the threshold of the device drive it into deep depletion, causing V_t instability. This points out a weakness of the multiplexed circuit, in that the exact OFF-state voltage at the gate of the HVTFT is difficult to control due to feedthrough effects from the parasitic capacitance of the LVTFT pulling the gate of the HVTFT low. This "Hard OFF" condition is exacerbated by the upwardly shifting thresholds of both devices due to the aforementioned equilibration effects. Fortunately, with the use of a field plate, the desired uniformity and low ON-voltages can be achieved, the V_t shift can be suppressed sufficiently to reach the desired uniformity. Fig. 19 shows histograms of the distribution of output low voltages for two 12-in electrographic print arrays, both arrays have been stressed for 3 weeks. The distribution on the right comes from an array without benefit of the field plate, the left distribution shows the output low voltages for a print array with field plates, both arrays have 200 drivers/in. As can be seen, the field plate gives the desired tight (all drivers within 8 V) distribution and the desired low voltage (mean = 4 V).

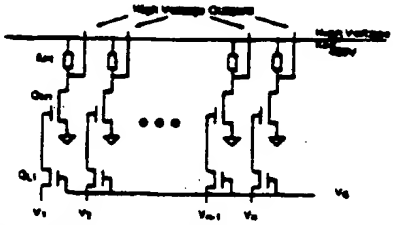

Fig. 18. Multiplexed circuit with high- and low-voltage TFT's.

One final circuit consideration with the HVTFT device is due to its high gain. For the circuit of Fig. 18, adequate enable times (or "gate times") for charging and discharging the HVTFT are on the order of 15 to 25 μs. However, the turn-off time constant of the HVTFT (assuming a 1-GΩ pullup and a 0.1-pF output capacitance) will be on the order of 100 μs. The gate-to-drain capacitance of the HVTFT, although reduced due to the offset gate structure, is still on the order of 0.1 pF and is sufficient to cause a sizable Miller effect. Since most of the rise of the HVTFT drain occurs after the gate time, the rising drain potential pulls the HVTFT gate high enough in potential to stop the OFF transition. Thus the HVTFT is not turned completely off by a single write pulse. This problem can be overcome by going to longer gate times. However, an elegant solution exists through the use of a cascode circuit, depicted in Fig. 20. In this case, the HVTFT is switched by the series combination of the HVTFT Q_H and the LVTFT Q_S. Through current matching, the HVTFT can be switched by charging and discharging the gate of Q_S though the pass TFT Q_P. This circuit eliminates the Miller effect by completely isolating the large voltage swings of the HVTFT drain from the storage capacitance of the of Q_S's gate. The current-matching condition in the OFF-state, however, can cause the source of the HVTFT to reach high enough values to cause large V_t shifts if the HVTFT has higher leakage current than the LVTFT. This problem can be easily overcome through the used of a small region of ungated a-Si current in parallel with Q_S. This ungated Si ensures that the HVTFT (in the OFF-state) will always be biased at a point below threshold, since the current through it will be determined by the space-charge-limited current through the ungated silicon. But above a "Hard OFF" condition since the current through the ungated Si will be greater that the leakage of

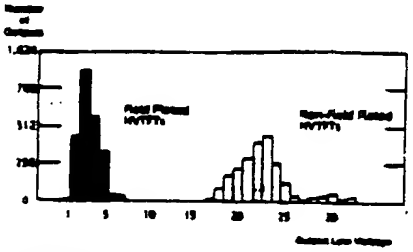

Fig. 19. Distribution of output low voltages for inverter arrays using HVTFT's with and without field plates.

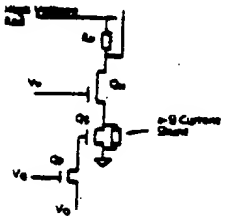

Fig. 20. A high-voltage output driver circuit using the cascode configuration.

either device. This circuit solution also provides greater V_t stability since the current matching characteristic setup by the ungated Si will always ensure an OFF condition at a point just below threshold, even as the thresholds shift to higher values with use.

X. Summary

A technology for HVTFT's has been described. Instabilities in I_D–V_D, described by the parameter V_t, arise from the creation of locally higher density of states. This instability can be controlled by the structure of the HVTFT and is very much reduced by the addition of a positively biased field plate. The performance has been described in terms of both an analytical and numerical model. Application of HVTFT's to output driver circuits has been given.

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